Flat Contacts for Carbon Nanotube Circuits

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ABSTRACT

We attempted to construct flat contacts for carbon nanotube circuits using a mechanical polishing process. These contacts were built on an oxidized silicon wafer by etching trenches in the oxide surface. These trenches were then filled with Au and polished down to nanometer flatness. It is hoped that these contacts will allow us to assemble molecular circuits in a controlled manner.

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1. Introduction

Carbon Nanotubes are a new type of carbon molecule, and look like rolled up graphite sheets (*fig. I*). Discovered as reaction by-products in C_{60} synthesis, they possess remarkable electrical and mechanical properties. Whether a tube is a metal or a semiconductor is determined by its geometry, and the Young's Modulus of nanotubes is predicted to be up to 100 times that of steel [1].

The physical dimensions of nanotubes are impressive as well. A single walled carbon nanotube is approximately 1.4 nm in diameter, but its length can be on the order of microns. This aspect ratio, on the order of 10,000, is virtually unheard of on a macroscopic scale.

The single walled carbon nanotube (SWNT) described above is but one form of nanotube. Multi-walled tubes (MWNT) exist, and SWNTs are sometimes observed to coalesce into "ropes", bundles of tubes which can contain anywhere from a few up to several hundred tubes [2]. Bundles of these ropes can come together to form structures as long as a few tenths of a millimeter. This indirect bridging of microscopic and macroscopic length scales has interesting consequences.

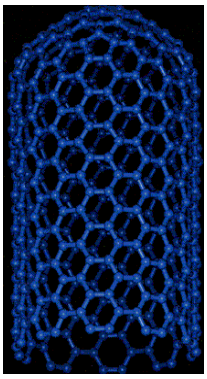
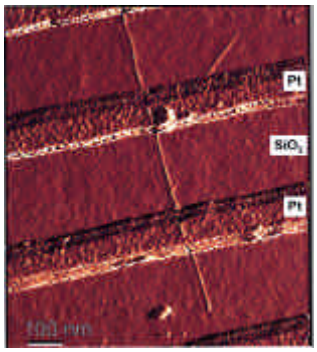


Fig. I – Structure of a Carbon Nanotube

The electrical properties of nanotubes, along with their micron-lengths, affords us a unique opportunity. With electron beam lithography, it is possible to create metal leads much smaller than one micron. This, coupled with the fact that nanotubes can be metals, gives us the ability to achieve true molecular electronics. The issue of how to connect macroscopic contacts to microscopic molecules is an extremely difficult problem and is the single biggest impediment to molecular manipulation. Because nanotubes are huge molecules with metallic character, we can manipulate them and make macroscopic connections to them.

It has already been shown that nanotubes can be used to make electrical devices. In May 1998 a group at Delft Institute of Technology fabricated a molecular transistor which operated at room temperature [3] *(fig. II)*. Diodes have been fabricated as well, and research on nanotube-nanotube contact resistance is underway [4].



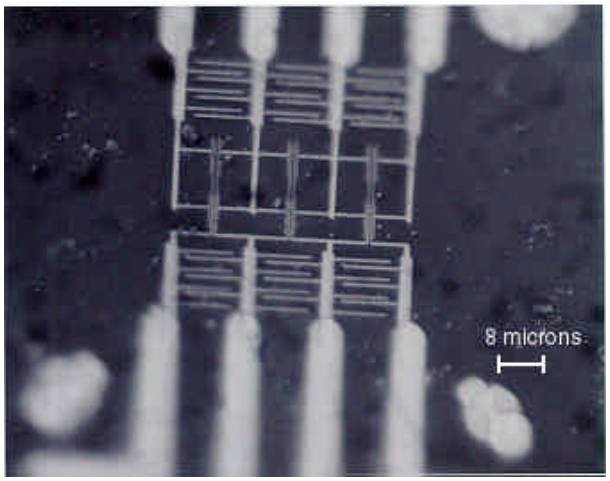
The problem with present work on nanotube electronics is that results are not reproducible, and it is impossible to make circuits with more than one tube. The standard method for making these devices leaves much to chance. After metallic leads are constructed, the tubes are spun on. In doing this, one hopes a tube will lie across two of the leads. While this method is good for proof-of-concept, it cannot be controlled.

A technique has been developed at the University of Pennsylvania for moving tubes on a flat surface using a tapping-mode Atomic Force Microscope (AFM) [5]. This method has been highly successful at translating and rotating tubes, but its usefulness is limited in the present scheme, since it is not possible to push a tube onto a 30 nm high electrode. It is hoped that once flat contacts are constructed, we can use this technique to probe individual tubes and ultimately assemble circuits in a controlled and reproducible manner.

Further motivation for flat contacts comes from the fact that putting a tube on a raised electrode distorts the tube's shape, changing the tube's electrical structure. In extreme cases, tunnel barriers form. Such distortions are impediments to current flow and are not easily controllable.

The efforts to build these contacts have focused on two methods. They are "Sacrificial Substrate" and Trench Filling / Polishing. Both are described below.

For Sacrificial Substrate, a pattern of wires was deposited on a silicon wafer. On top of this went an etch stop layer, and above the etch stop was glued a glass slide. The sample was then put in a 7.14 Molar KOH solution at 52 ^{o}C . This solution dissolves silicon. After the silicon is etched away, flat metal contacts should be exposed. The details of this process are described in section 2.1, and a discussion of the results follows in 3.1 . This method was not successful.



the center of fig. III .

Here we present the two methods, and defer detailed discussion to section 3.

2.1 Sacrificial Substrate

The steps of the sacrificial substrate process were as follows (*see fig. V*):

1) Deposit an Au pattern on a (110) silicon wafer[*].
2) Put an etch-stop layer on top of the Au.
3) Glue a glass slide on top of the etch stop layer.
4) Etch Si substrate away at 14 μm per hour in a 7.14 Molar KOH etching solution at 52 ^{o}C . The silicon wafer is 300 +/- 25 μm thick, so it is etched for roughly 21 hours.

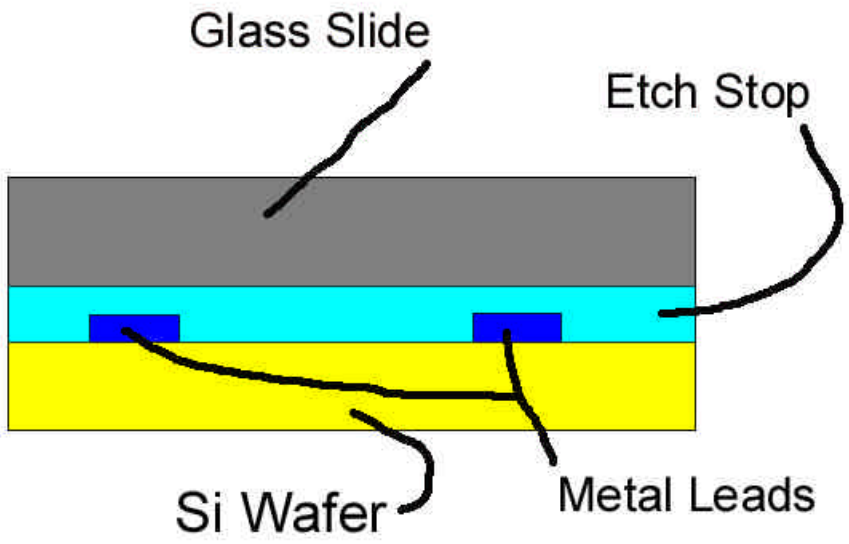


Fig. V – Sacrificial Substrate Process. This assembly would be flipped over after the Si is dissolved and before we spin on tubes.

After the silicon is dissolved, the etch stop halts the advance of the KOH. What should be left are metal contacts which are flat with the sample surface. As described in section 3, this method was unsuccessful, and flat contacts were never observed.

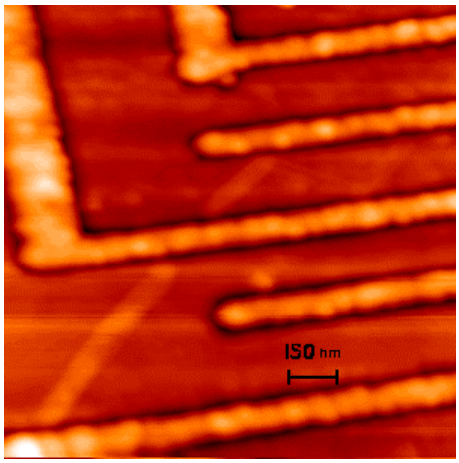
2.2 Trench Filling / Polishing

Trench filling was initially attempted by Marko Radosavljevic[6]. The process used the first time was as follows:

[*] Normally when depositing Au on Si, an adhesion layer of Cr is used, since the Au does not stick to Si well. It was not possible to use an adhesion layer here. After the silicon was dissolved, the underside of the pattern was exposed. If an adhesion layer had been used, this would have been exposed.

1) Make a pattern on an insulating substrate using lithography
2) Etch trenches in the sample with a plasma process
3) Evaporate metal into the trenches and do lift off (see appendix C)

The problem with this process was undercutting. The plasma etch used was isotropic, which means it etches equally fast in all directions. The result is that after lift-off, there are holes next to the metal leads (fig. VI)



To overcome the problem of undercutting, this process was used:

1) Make a photolithographic pattern and etch 100 nm deep trenches in silicon dioxide. For this a different isotropic etch, buffered hydrofluoric acid, was used.
2) After etching the trenches, strip off all photoresist.
3) Evaporate metal (~50 nm into the 100nm trench[†]). Because the photoresist was stripped already, metal is evenly applied on the bottom of the trench. The undercut holes are eliminated.
4) Mechanically polish the sample. The idea is that the Au on the unetched SiO_2 surface is removed first and the Au in the trenches remains. The sample is then scanned in the Atomic Force Microscope (AFM) to determine the exact distance between the tops of the trench and the metal.
5) The AFM data tells how much oxide must be removed to make our substrate flat with the contacts. The removal rate of thermally grown oxide is already known (appendix B). It is then possible to remove excess oxide and form the flat contacts.

[†] The trenches are underfilled in this step. The reason is so when oxide is removed, the polishing doesn't touch metal in the trench. Oxide is removed until the surface is level, and then the polishing stops. If polishing the metal can be minimized, damage to our pattern can be minimized. Compare the scratching in fig. XI (underfilled) to fig. VII (completely filled trenches).

Fig. VII Pattern damage in completely trenches

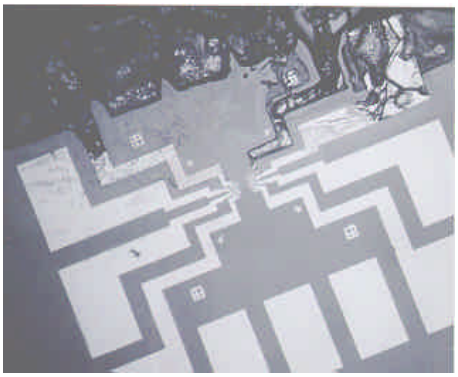
One more method is being investigated in addition to the polishing process described above. For this, metal wires are deposited photolithographically on an SiO_2 substrate. We then evaporate another layer of SiO_2 on top of the gold leads. It is then polished down until the SiO_2 is removed from the surface of the leads. This process is in too early a stage to comment on its viability.

3. Discussion and Results

Superior results were obtained with the trench filling process. In every implementation of Sacrificial Substrate, the Au-silicon interface was attacked and the metallization damaged.

3.1 Sacrificial Substrate

This technique was implemented numerous times with a variety of materials. It was hoped that as we approached the end of the etch, thin film effects would cause a color change in our sample. This was not observed, and in all cases the etchant was able to seep under the sample and destroy the pattern (*fig VIII*).



Etchant attacks Metallization. In all the samples tested, KOH seeped into the Au-silicon interface and destroyed the metallization.

3.2 Trench Filling / Polishing

To overcome the undercutting problem (see appendix A), we did lift off on the adhesion layer. The sample was then returned to vacuum and a 30 nm layer of Au deposited over the entire surface of the wafer. The result is Au which has good adhesion at the bottom of the trenches and poor adhesion at the top, and a 50 nm gap between it and the top of the trench. The Au on top of the trenches can then be removed easily by polishing with colloidal silica.

Once the Au is removed from the tops of the trenches, the sample will be sonnicated (cleaned in an ultrasound water bath) to remove silica particles, cleaned with acetone, and scanned with the Atomic Force Microscope to determine the exact depth of the trenches (in the underfilling scheme).

At this point in the processing, our sample will consist of metallized contacts at the bottom of 50 nm trenches. After determining the trench depth, the sample will be polished. The tops of the trenches will be metal free, and can be polished down with colloidal silica. The removal rate of the oxide has been experimentally determined to be 2.5 +/- 0.9 nanometers per minute (see appendix B).

This process has not yet progressed past mechanical lift off. However, encouraging data have been gathered about the flatness of the post-polish oxide regions. AFM scans of polished samples indicate that the oxide is flat to within a few nanometers (*fig. IX*). It is therefore extremely likely the contacts be flat enough to use with nanotube circuits.

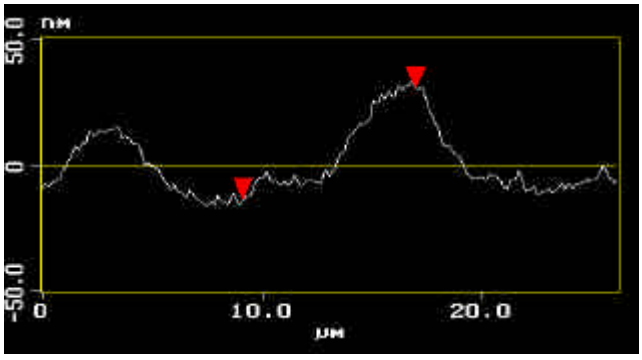


Fig. IX – Cross section of the polished oxide. Observe the flatness of the plateau regions (note the scales).

4. Conclusions / Discussion

Although the sacrificial substrate technique did not yield the desired results, trench filling has shown itself to be a promising candidate. Underfilling will hopefully produce flat contacts. It delivers sharper features and less metal damage than complete filling (compare figure VII to figure X).

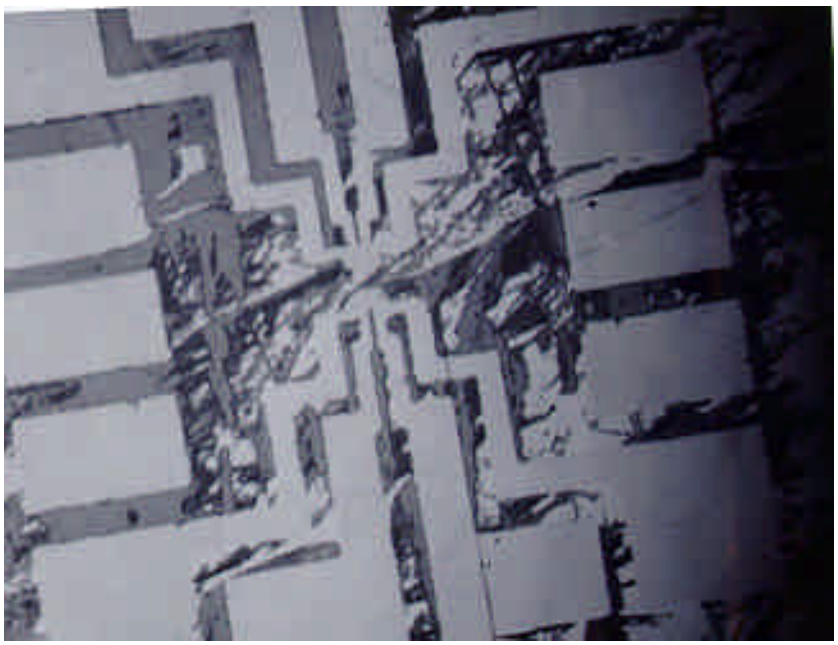


Fig. X – Underfilled Trenches. Note how the pattern is much sharper than the completely filled trenches (fig. VII). Also, the underfilled sample doesn't have as many scratches on its leads.

We have not tried the other polishing process (polishing evaporated SiO_2) enough to comment on its viability. This method is being developed in parallel with trench filling, and its usefulness will be determined in the near future.

Once flat contacts are manufactured, mainstream molecular electronics will be closer to reality. The degree of control allowed by these contacts opens the door for industrial applications, and they may be used as a stepping stone to probing even smaller molecules. Just as researchers have used lithography to produce nanotube probe stations, one could conceivably use the nanotubes to study more elusive molecules. As Richard Feynman once said, "there's plenty of room at the bottom", and these flat contacts are a crucial step in this direction.

5. Acknowledgements

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6. References

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The etchant removes material in the sideways directions in addition to down. However, the photoresist used here as a mask is not removed. After etching, it overhangs the edge of the trench, and the deposited will not get into the undercut areas.

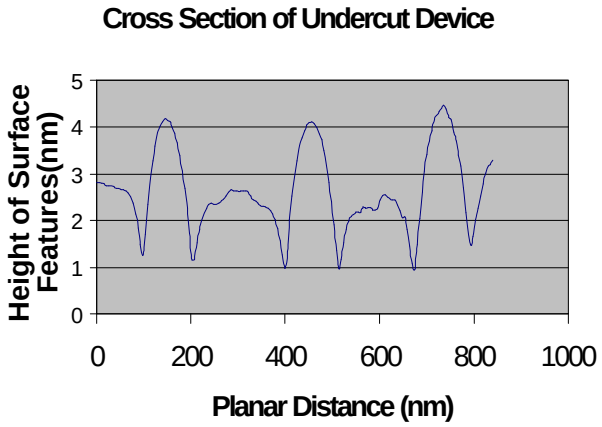

Figure A.II – Cross Section of Undercut Electrodes

Figure A.II is a topographic cross section of the device obtained using the Omicron SPM Data. The three large, even peaks we see are three electrodes. Each electrode is flanked on either side by a hole, the “

Appendix B
Determining the Oxide Removal Rate

To properly control the polishing process, it was necessary to know the removal rate of the thermally grown silicon dioxide. To determine this, 50 nm trenches were etched in a 200 nm layer of oxide. One sample was scanned in the AFM to determine the actual trench depth (the control sample) and the remaining five samples were polished on an Allied High Tech TechPrep 8 with micro-positioning head. 0.02 micron colloidal silica polishing slurry was used, as well as an extremely fine polishing pad (Allied High Tech Chem-Pol PSA Back Polishing Cloth).

The other five samples were polished at 25 rpm for 5s, 30s, 1 min, 5min, and 10 min. Each sample was impressed 10μm into the pad, except for the sixty second sample (impressed 30μm. The removal rate was so slow that the 5 and 30 second samples yielded no useful data (the removal rate was 2.5 +/- 0.9 nm/minute, and the uncertainty in our measurement of the trenches was on the order of +/- 3 nm). The one minute sample (impressed 30μm) was so heavily eroded that no useful data could be obtained from it, attesting to the important contribution of polishing pressure.

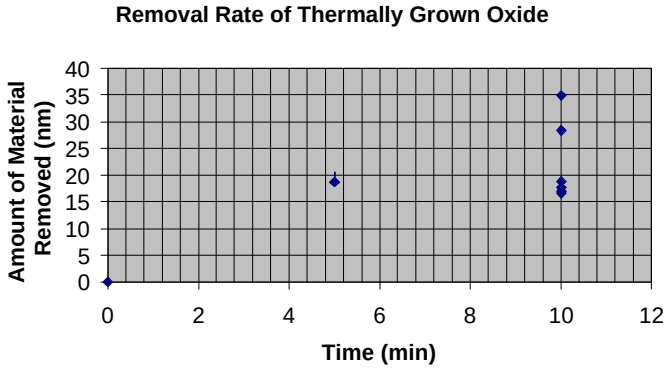

Fig. B.I

This is the raw data collected on the oxide removal rate. Examination of the data yields a removal rate of 2.5 +/- 0.9 nanometers per minute.

Appendix C – Lift Off Process

Lift off is a way to deposit metal onto a specific region on a silicon wafer. The steps for lift off are:

1) Spin on photoresist
2) Transfer a pattern to photoresist
3) Deposit metal evenly all over the sample surface
4) Dissolve the resist. When the resist goes, it takes with it excess metal, leaving it only in patterned regions.

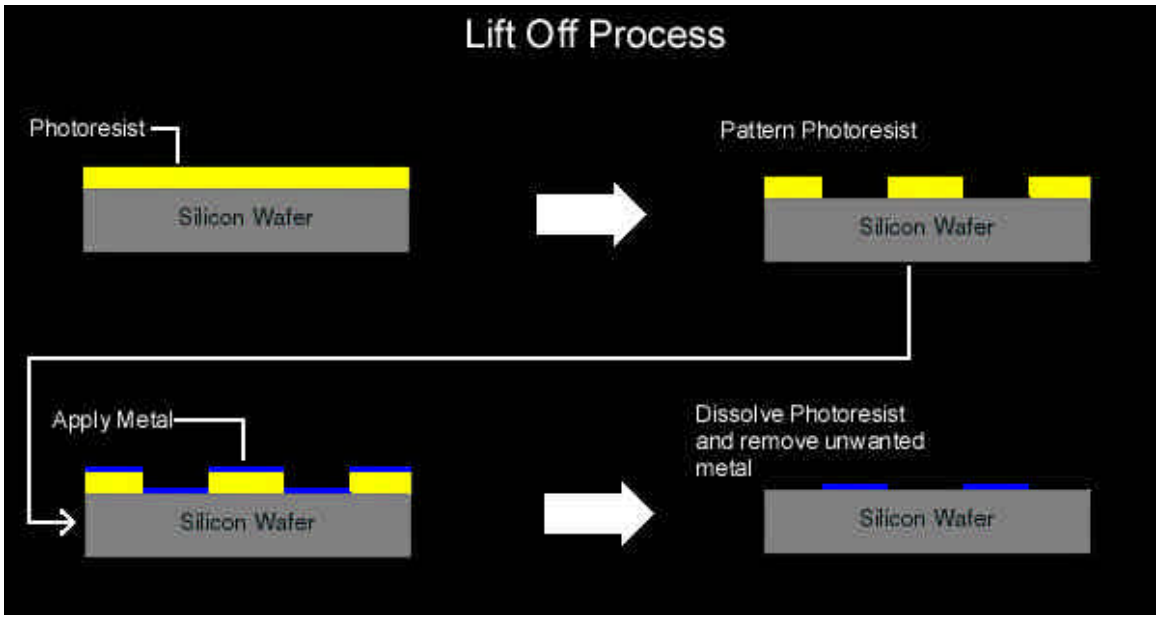

Fig. C.I – Lift Off Process