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DIELECTROPHORETIC ASSEMBLY, INTEGRATION, AND CHARACTERIZATION OF FUNCTIONAL NANOSTRUCTURES

NSF Summer Undergraduate Fellowship in Sensor Technologies
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ABSTRACT

Nano-electro-mechanical systems (NEMS) are pivotal to integrated systems research. The ability to integrate sensors and processors on a single wafer has the potential to create highly sensitive and complex systems that respond to changing environmental stimuli. This project focuses on the assembly, integration, and characterization of both nanowires and nanotubes used in NEMS devices. Using dielectrophoretic assembly, the project assembled and electrically characterized Rh and GaAs nanowires as well as multi-walled carbon nanotubes (MWNTs). It also found optimum parameters for assembly for each of these nanostructures for a specific circuit design. The optimum conditions always involved applying a sinusoidal field of 100 kHz at an amplitude of 10 to 35 V. The duration of assembly varied from 1 minute to 5 minutes. The capacitive properties of contact pads play a critical role in assembly yields, and resistivity of MWNTs is inversely related to temperature. The research also raised questions about the physical structure of these nanostructures and how it may be affected by changing temperature. It appears that a critical temperature is reached at which the resistivity of the nanotube increases drastically. Finally, the project produced clamped MWNTs for future mechanical testing.

Table of Contents

1. INTRODUCTION

Micro-electro-mechanical systems (MEMS) are perhaps at the forefront of integrated systems research. MEMS devices hold the possibility of integrating processing power and sensing power to create powerful micrometer-sized systems [1]. Thus MEMS devices have the potential to both sense and act upon environmental stimuli. These small-scale, fully functional devices could solve problems ranging from detecting diseases within the human body to exploring remote worlds. Furthermore, because their manufacturing processes are similar to integrated circuit techniques, MEMS devices can achieve a high level of durability, reliability, and complexity with relatively low costs.

MEMS research has the potential to revolutionize integrated systems research even further with the introduction of nanotechnology. Nanotechnology, or the manipulation and ordering of particles on the nanoscale, has numerous uses in a wide variety of fields. Specifically, for MEMS research nanotechnology has the potential to create even more advanced and smaller "laboratories on a chip." Nanoscale MEMS devices, known as NEMS (nano-electro-mechanical systems) devices, would be able to integrate numerous sensors, actuators, and processing units on a single silicon wafer.

Recent advances in the synthesis of nanowires (wires of some nanometer diameter) have given rise to the notion of creating rudimentary nanowire-based MEMS devices. To build these nanoscale devices, however, the physical, chemical, and electrical properties of the nanowires must be observed. Furthermore, their integration with micrometer-sized devices is pivotal to their commercial use. Hence, current research revolves around the characterization of these nanowires and their integration with their micrometer-sized counterparts (nanowires serve as interconnects between micrometer-sized features).

This paper is concerned with the assembly and characterization of certain nanoscale devices. Specifically, this paper reports on Rh nanowires, GaAs nanowires, and multi-walled carbon nanotubes (MWNTs). The rhodium nanowires are metallic structures that should act as conductors. The GaAs nanowires are semiconducting structures that are expected to have a specific band gap, one that could lead to applications in optics [2, 3]. The MWNTs can be used as a mechanical device to transport fluid. They also have applications as a field emitter, sensor, and battery electrode [4, 5].

This paper will first give a brief literature review, describing how these nanostructures are synthesized and assembled. The review discusses the laser-assisted catalytic growth process, the most popular method for synthesizing nanowires; various methods for synthesizing the carbon nanotubes, including chemical vapor deposition, the most popular method; and various ways to assemble these nanostuctures, culminating in dielectrophoresis. Dielectrophoresis was the process used in this research. This report details the assembly of these three nanostructures, giving the optimal conditions that should be used to assemble them on metallic electrodes. The equipment and process used to trap these structures in places where they were easy to characterize are described.

The next section of the report discusses how the nanostructures were characterized — specifically, current-voltage relationships and how they change with temperature. This information is important so that these structures can be characterized as sensors. The paper concludes by discussing ways in which the research could have been improved, ideas for future research, and the broad outlook for the future of NEMS devices.

2. LITERATURE REVIEW

2.1 Nanowire Synthesis

Nanowires and nanotubes can be synthesized and assembled in a variety of ways. Scientists and engineers are continually trying to develop new methods to give people more control over the outcome, including how long and wide these nanostructures should be and where they assemble on very large scale integrated (VLSI) circuits.

A popular way to synthesize nanowires has been developed by scientists at Harvard University [6, 7]. This method, called laser-assisted catalytic growth (LCG), uses a vapor-liquid-solid process. The process was first used to synthesize Si nanowires. In this instance, the process began with a solid piece of $Si_{0.9}Fe_{0.1}$. Laser ablation of the Si-Fe combination created a vapor of Si and Fe that quickly condensed to form liquid Si-Fe nanoclusters. These nanoclusters acted as the catalyst upon which the nanowire was grown. The nanoclusters were then supersaturated in Si, which then precipitated and crystallized as nanowires.

The success of this process requires consulting a binary phase diagram for Fe-Si. This phase diagram can show where FeSi liquid can coexist with a Si solid. The process should then be operated at this temperature and pressure so that the FeSi liquid catalysts can start the crystallization of Si nanowires. For this reason, to create Si nanowires on a FeSi catalyst, the experiment had to be run above 1150°C. While this was not impractical, it was desirable to find a lower temperature [6, 7].

Gold and silver have been studied as possibilities for creating a nanocluster catalyst. Inspection of the Au-Si binary phase diagram indicated that creating Si nanowires from an Au catalyst could be done nearly 800°C lower than when using Fe. In this case, however, the nanoclusters would consist of pure Au and not an Au-Si combination as when using Fe. Experiments demonstrated that Si nanowires grew on Au catalysts at temperatures between 370°C and 500°C. Furthermore, the nanoclusters that terminated the wires were indeed Au [6].

While this method was easily extended to create Ge nanowires, creating compound semiconducting nanowires proved to be more complicated. Compound semiconductors, such as GaAs, create a more complicated phase diagram because there are now three elements to consider: Ga, As, and a metal used for the catalyst (usually Au) [8, 9]. The phase diagram was simplified, however, by looking at the pseudobinary phase

diagram of the metal and the semiconductor. In this case, the compound semiconductor was treated as a single element. By using this method, researchers could synthesize GaAs nanowires on Au nanoclusters at temperatures above 630°C.

Finally, the length of the nanowires can be controlled by the time spent at higher temperatures. As long as the nanowires are in the furnace, they will continue to grow. They will leave the furnace when the gas flow from the laser ablation carries the wires out of the furnace. The laser ablation can be controlled; thus, the length of the nanowires can be controlled and predicted [6].

Thus, the laser-assisted catalytic growth method for synthesizing nanowires is quite useful. Known phase diagrams can be used to accurately predict optimal conditions for synthesizing the wires, and laser ablation can be used on a variety of metals to create catalysts.

2.2 Carbon Nanotube Synthesis

Because carbon nanotubes are different from nanowires, a different process of synthesis is needed. Nanotubes are hollow structures through which liquid could flow. Nanowires, on the other hand, are solid structures that will conduct current and can otherwise act as a wire. Synthesizing a tube proved to be more difficult, though the process was similar.

2.2.1 Carbon Arc Discharge Method

Carbon nanotubes were first discovered by accident by Sumio Iijima. The accidental conditions were then reproduced in an effort to purposely synthesize the nanotubes [10, 11]. A DC voltage of approximately 20 V was applied to pure graphite electrodes. The current was kept between 40 and 100 A. These conditions caused an electric discharge between the anode and the cathode. This discharge creates a carbon plasma, and the anode is constantly evaporated and deposited on the cathode.

The deposition on the cathode forms a cylindrical shape that can then be broken off and opened. Inside are numerous columns that contain nanotubes. These tubes form only when there is a large amount of current (40 A or higher). If there is not enough current, the deposits will simply be amorphous carbon.

This process is not very accurate and leaves little control over the size and length of the nanotubes. It also gives little control over where they are synthesized. A new method, known as chemical vapor deposition (CVD), uses the same basic idea of depositing a carbon plasma, but attempts to control the outcome more than the electric discharge method.

2.2.2 Chemical Vapor Deposition

A method employed by chemists at Nanjing University in China uses a process called microwave plasma-enhanced chemical vapor deposition (MW-PECVD) [4, 5]. This process is similar to LCG because it uses a catalyst to grow the nanotubes. In this specific experiment, the Fe was used as a catalyst to grow the carbon nanotubes. The catalysts were placed in a quartz tube, which was then placed in a vacuum system. Argon and hydrogen were first used to reduce the Fe catalysts, and then benzene vapor was introduced into the system. The benzene vapor then crystallized on the Fe catalysts, forming nanotubes.

The MW-PECVD system was improved in South Korea at Chungnam National University. The deposition of metal films in a vacuum was replaced by a spin coating of a magnetic field solution. The magnetic fluid was created by dispersing magnetic nanoparticles in solution. The solution used was a dispersion of Fe_3O_4 nanoparticles dissolved in ammonia hydroxide. It was coated on a Si wafer and then placed in a furnace under low pressure. NH_3 gas was introduced into the furnace followed by C_2H_2. Carbon nanotubes were formed on the Si substrate.

It was found that the diameter of the nanotubes was directly proportional to the diameter of the nanoparticles in the magnetic fluid. Larger particles yielded larger nanotubes. The researchers could control the size of the nanoparticles by the amount of ammonia hydroxide. A larger amount of the ammonia hydroxide yielded smaller nanoparticles, which then yielded smaller nanotubes. Since the diameter of the particles could be controlled easily, so could the diameter of the tubes.

2.2.3 Template-Synthesis Method

A completely different method for synthesizing carbon nanotubes uses templates. Scientists from Tsinghua University in Beijing have developed a technique that uses templates to control the diameter of the nanotubes [12].

They use highly ordered anodic aluminum oxide (AAO), which is a nanoporous material. The size of the pores can be controlled by adjusting the oxidizing voltage of the aluminum. The AAO was placed in a vacuum chamber, and CVD was used to synthesize the nanotubes within the pores of the AAO template. Iron was used as a catalyst and was electrodeposited into the pore bottom of the template. The Fe was then reduced, using hydrogen gas, and an ethylene-argon gas mixture was introduced into the system. The nanotubes then grew on the Fe catalysts that had taken the shape of the pores in the AAO template.

The diameters of the tubes were directly proportional to the diameters of the pores. The average diameters of the tubes were generally a few nanometers larger than the diameters of the pores, but this is thought to be due to thermal expansion of the pores during nanotube growth.

2.3 Assembly Technologies

This section describes previous methods used to assemble nanowires. In this section, three specific methods will be described: directed growth, chemical templating, and dielectrofluidic assembly. It will review the works of Dr. Hongjie Dai (Stanford University) on directed growth procedures, Dr. Chad Mirkin (Northwestern University) on chemical templating, and finally Dr. Thomas Malluok (Penn State) and Dr. Theresa Mayer (Penn State) on dielectrofluidic assembly.

2.3.1 Directed Growth

Directed growth is the method by which nanowires are grown at specific locations to integrate them with some other circuitry. This gives rise to the possibility of creating nanowire based electronic devices. Specifically this involves knowledge of nanowire synthesis using chemical vapor deposition. Chemical vapor deposition (CVD) is the process by which elements in gaseous form can be condensed to thin films of solid form. These thin films can then be deposited on a wafer. Currently, it is possible to grow Single Walled Nanotubes (SWNT) using a process known as catalyst patterning. Catalyst patterning is similar to standard photolithography procedures for wafer fabrication, except that an additional catalyst layer is placed on top of these electrodes [13, 14, 15, 16]. This catalyst layer contains special chemical properties that allow CVD processes to actually orient and grow SWNTs across these electrodes.

After initial wafer fabrication is complete (using standard photolithography / thermal oxidation / sputtering procedures), "a poly(dimethylsiloxane) (PDMS) elastomer stamp"[pg. 7975, 14] is covered with a catalyst solution. This PDMS stamp is then placed on top of the fabricated wafer, hence transferring the catalyst solution to the electrodes on the wafer. After calcinations, the wafer is run through standard CVD processes. This causes the growth of the SWNTs across the electrodes on the wafer.

Using this catalyst / CVD method (catalyst patterning), growth of rudimentary nanostructures is possible. The key to growth is the catalyst material used and the conditions of the CVD processes. Furthermore, wafer fabrication also plays an important role in SWNT growth. Gaps between adjacent electrodes affect lengths of the grown SWNTs [15,16]. Also, using directed growth, a strong bond between electrode and SWNT is present. This is useful when doing mechanical testing on the grown SWNT.

2.3.2 Chemical Templating (DNA Templating)

Chemical templating is a process by which nanoparticles can be assembled using the recognition patterns of DNA. By using thiol modified nanoparticles, a DNA pattern can be added within them. Hence, when another thiol modified nanoparticle is introduced that complements the first one, assembly occurs. This section will examine the work of Dr. Chad Mirkin in this field.

DNA templating, as a method for nanoparticle assembly, is employed by doing the following. First, nanometer sized particles (such as Au) have attached on their surfaces DNA oligonucleotides and thiol [17]. Thiol is used as an adhesive between the Au particles and the oligonucleotides. When nanoparticles with complementary DNA oligonucleotides are introduced, assembly occurrs. Thermal denaturation is the process by which one can disassemble these particles.

Furthermore, two component nanoparticle systems can also assemble by DNA templating [18]. A component is a reference to a specific type of particle; Au specifically was used in Dr. Mirkin's one component system. Similar thiol based particles are used once again for templating in the two component system. This shows that DNA templating based assembly is not necessarily subjected to a particle's size and chemical composition. Hence, it gives rise to the possibility of constructing "anatural" bondings and having different types of particles assemble (e.g. Au and Rh).

2.3.3 Dielectrofluidic Assembly

Dielectrofluidic assembly is the method used by this project to assemble nanowires. Dielectrofluidic assembly involves the introduction of electric fields to assemble nanowires suspended in some medium (such as acetone or isopropanol). This assembly procedure involves the optimization of three parameters, voltage, time, and frequency, to maximize nanowire assembly yields. This section will look at the papers of Dr. Thomas Malluok and Dr. Theresa Mayer.

This method begins with lithographically defined electrodes where nanowires can assemble. For electric field assisted assembly to occur, metallic nanowires must polarize [19]. The most convenient way for polarization is through the introduction of an AC signal source. This is due to the source's frequency. Usually, a higher frequency allows the nanowires to polarize more quickly. The unfortunate fact of this is that too high of a frequency actually causes no polarization and consequently no assembly. It should also be noted that once a nanowire assembles, the possibility that another nanowire will assemble near it is low. This is due to the assembled nanowire's own electric field impeding further assembly.

Another parameter that decides assembly yields for this method is the peak to peak voltage applied by the AC signal sources [19,20]. A higher peak to peak voltage causes a stronger electric field. Hence, with stronger electric fields, there is greater likelihood that a nanowire will assemble. However, like the frequency parameter, too high of a voltage causes the assembly electrodes to actually burnout.

Lastly, the time the AC signal source is present is also important in determining assembly yields. Much like the voltage parameter, the time the AC signal source is present has a direct effect on the chance for assembly. However, again like the voltage parameter, too great of a time can actually cause the assembly electrode to burnout. This is due to the fact that the assembly electrodes are just capacitors, and hence, when the dielectric medium between them (air) becomes conductive, a short is produced.

3. EXPERIMENTAL METHODS

3.1 Wafer Design

The wafer design process involved the development of two distinct designs for different uses. The first design, the experimental wafer design, was created primarily for the University of Pennsylvania's NEMS Laboratory. It served as a vehicle for both nanowire assembly and testing. The second design, the VT / Experimental wafer design, had dual purposes. Because the design was outsourced to locations with greater precision than the University of Pennsylvania's Microfabrication Laboratory, more sensitive versions of the first design were produced. Along with the more precise version of the first design, the VT / Experimental design also had a replication of a VLSI Virginia Tech design, which at a future date, could serve as another testing vehicle for the NEMS Laboratory. The experimental wafer design was actually fabricated, while the VT / Experimental design was completed only up to its design stage.

3.1.1 Experimental Wafer Design

The goal of this wafer design was to create a wafer that could assemble nanowires and test them for electrical and mechanical properties. Electrofluidic assembly was the method used for assembly. Electrofluidic assembly involves the introduction of electric fields to assemble nanowires suspended within some solution (usually acetone or isopropanol). The design used micrometer-sized conductive electrodes (see Figure 1) for AC signal source excitation. This created a uniform electric field between these electrodes. However, an electrically insulating SiO_2 layer was added on top of the now "buried" electrode layer, to create a weakened electric field above the SiO_2 layer. The design then added another conductive electrode layer on top of the SiO_2 to concentrate the weakened electric field between these "upper" electrodes (passive electrodes). This concentration of electric field makes it possible for nanowire assemblage to occur on this wafer, given the proper voltage, frequency, and time parameters for the AC signal source.

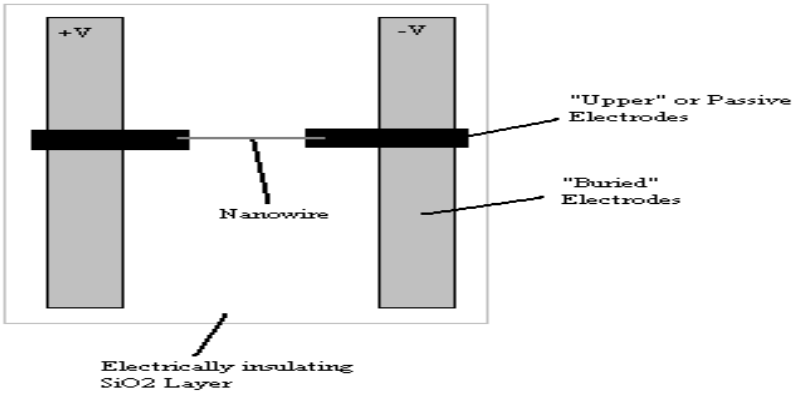

Figure 1. Experimental design setup.

All designs for the wafer were done using AutoCAD 2000 software. The wafer model was a 4-layer design with 100 assembly sites (places where nanowires could assemble) per circuit. Two different designs, "clamped" and "unclamped," were placed on the wafer, and this section will elaborate on their characteristics.

Circuit designs for both the "clamped" and "unclamped" versions began with the "buried" electrode layer. This layer was the site for the AC signal source introduction. The layer is considered "buried" because it is the first layer on the wafer and consequently underneath layers 2, 3, and 4 (see Figures 1 and 2). All electrodes within this layer were of 10 μm width. This layer provides 10 pairs of parallel electrodes, with one of the pairs connected to the positive signal source and the other to the negative signal source. Each of these parallel electrodes was 500 μm long. Additionally, this layer provides two electrodes that connect the paired electrodes to outside AC signal sources. Other lengths are specified in Figure 3.

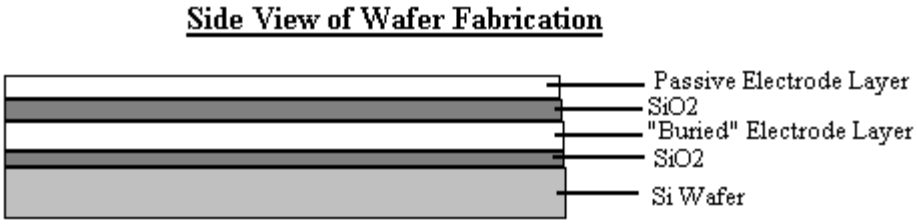

Figure 2. Side view of wafer fabrication (thickness not to scale).

The second layer for both "clamped" and "unclamped" versions provides contact points between the aforementioned "buried" electrode layer and the third layer. As stated before, after the "buried" electrode layer (layer 1) is added, layer 2 is the electrically insulating SiO_2 layer. Since layer 2 is electrically insulating, it is not possible for any outside AC signal source to induce an electric field on the "buried" electrode layer. Hence layer 2 of the AutoCAD model etches out 50 μm-sized squares from the SiO_2 layer so that contact can be made with the "buried" electrode layer. Two squares are etched out — one for the positive and one for the negative AC signal source contact point.

The third layer for both versions is the "upper" electrode or passive electrode layer. This layer produces concentrated electric fields between all passive electrodes as a result of their conductive properties. These passive electrodes, coming in pairs (because one will take positive and one will take negative signal sources), are also known as assembly sites (see Figure 4). Spacing between each passive electrode pair varies from 5 μm to 30 μm (5 μm, 6 μm, 7 μm, 8 μm, 10 μm, 12 μm, 15 μm, 20 μm, 25 μm, and 30 μm) and changes per column (see Figure 3). These varying lengths allow for a multitude of different-sized nanowires to be assembled on a single circuit. All passive electrodes have widths of 10 μm.

The third layer also provides for vias, or contact pads where electrical probes can be placed to excite AC signal sources across the wafer. Using the inlets provided by layer 2 (which removes 50 μm squares from the electrically insulating SiO_2 layer), the

third layer encloses those inlets (allowing for contact with "buried" electrode layer 1) and then connects them to relatively large 200 µm squares. These 200 µm squares in the third layer serve as contact pads for electrical probes.

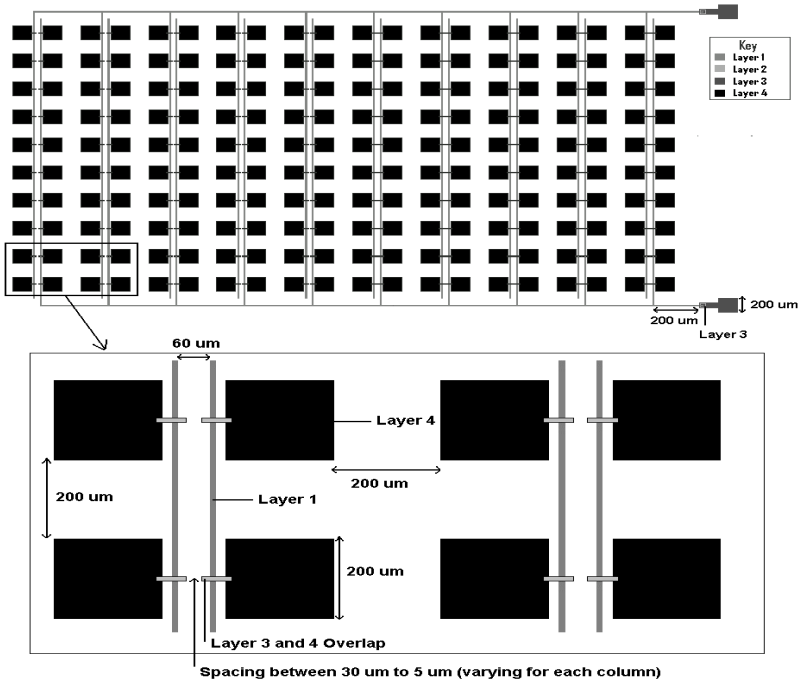

Figure 3. Experimental wafer design and dimensions.

Differences in the "clamped" and "unclamped" versions arise first in layer 3. Layer 3 is completed in the "clamped" version after all passive electrodes and vias are added. A "clamped" version is more useful in mechanical testing of assembled nanowires because this version essentially clamps down the nanowire after assemblage, and hence, provides for a more stable testing environment. The fourth layer for a "clamped" version circuit is introduced after electrofluidic nanowire assembly has occurred. This fourth layer goes on top of the passive electrodes and the assembled nanowire — so the nanowire is sandwiched with the third passive electrode layer on bottom and the fourth clamping electrode layer on top.

In the "unclamped" version, which is better used for electrical testing purposes, layer 3 also includes 200 µm-square contact pads, adjacent to and overlapping the passive electrode pairs. Measurements including I-V curves, resistance, and other properties can be obtained using these pads.

Layer 4 is applicable only to the "clamped" version of this circuit. As described before, layer 4 essentially sandwiches the assembled nanowire in order to create a more suitable environment for mechanical testing. Layer 4 also includes 200 µm-square contact pads for the same reasons as in the "unclamped" version. Dimensions and locations of layer 4's clamps are identical to those of the passive electrode layer in layer 3.

Several other factors were taken into account for this design. First, all points in the design where adjacent figures were to come into contact had to overlap. This took into account the possibility that fabrication mistakes could occur (e.g., electrical connections would hold even if there was a 1 μm mistake in fabrication). Second, all dimensions for all figures had to be revised to adhere to the University of Pennsylvania Microfabrication Laboratory's capabilities (i.e., smallest dimension of 3 μm). Finally, alignment marks and cutting marks were also present on the design to ensure proper layer alignment.

3.1.2 Virginia Tech / Experimental Wafer Design

Like the experimental wafer design described above, the VT design was created to assemble and test nanowires. All specifications in the first design could be scaled down because this second design will be outsourced to a location with more precise tools for fabrication. Additionally, a replication of a Virginia Tech VLSI design was added to this wafer. Both the smaller specification design and the VT VLSI design are discussed in this section.

Differences between the first wafer design and this wafer design are as follows. First, all assembly sites in the VT wafer have gaps ranging from 3 μm to 6 μm, with increments of approximately 0.3 μm, as opposed to gaps of 5 μm to 30 μm in the first design. Second, the VT wafer has a total of only three columns, as opposed to 10 columns in the first design. Hence there are only 30 possible assembly sites instead of 100. Finally, 16 of these circuits can be fit (due to their small size) on half of a 2 inch wafer.

The VT design is a VLSI design with a total of 17 assembly sites per circuit. Assembly sites on this design again vary from 3 to 6 μm, but with increments of 0.2 μm. There is a total of only one column and 17 rows in this design. The widths of all electrodes ("buried" and passive) are 3 μm.

There are three variations to the VT design. Design A of the VT design (see Figure 4) is a basic assembly circuit. Design B has its two 5 μm-wide electrodes (running parallel to the assembly sites) connected to the buried layer 1. These two parallel electrodes are connected to the 14 μm square but not to the assembly sites themselves. The parallel electrodes are used for testing a nanowire for electrical and mechanical properties after assembly. Lastly, Design C is similar to B except that it lacks the two 5 μm-wide parallel electrodes. This circuit is useful when connecting an assembled nanowire to a microprocessor for analysis.

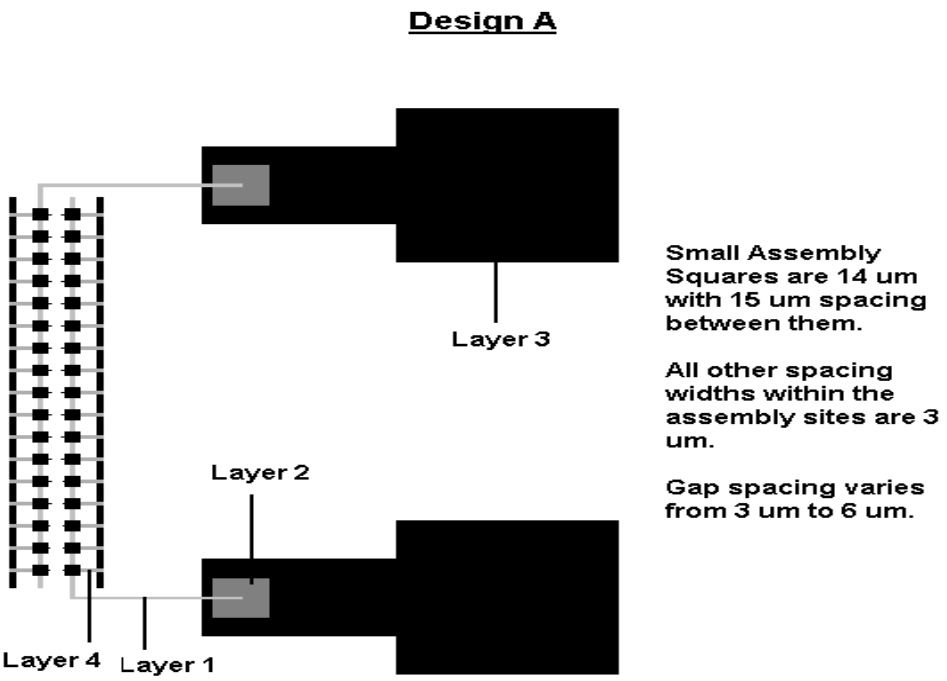

Figure 4. Design A of the VT design.

3.2 Wafer Fabrication

Fabrication of the experimental wafer involved three steps: mask fabrication, thermal oxidation / sputter deposition, and finally photolithography procedures. Each of these steps, along with the specifics of its application on these wafers, is explained in this section. This wafer fabrication involved only the experimental wafer design described in section 3.1.

3.2.1 Mask Fabrication / Photolithography

Mask fabrication involves the transfer of AutoCAD models into tangible glass plate patterns of a design. Masks serve as stencils for etching a design on a particular wafer . There are two types of masks: clear field and dark field. Each "paints" (adds) a layer on the glass plate that blocks UV light. Clear field masks "paint" the AutoCAD design on the glass plate. Dark field masks "paint" everything on the glass plate except the AutoCAD design.

These masks are important during photolithography procedures. Photolithography is the process of etching a design onto a particular layer, using UV light and photoresists. Photoresists, similar to photographic film, exhibit different chemical and physical properties when exposed to UV light. One of these properties, vulnerability to certain acids, is what allows a mask and photoresist to etch out a pattern within a layer (see Figure 5).

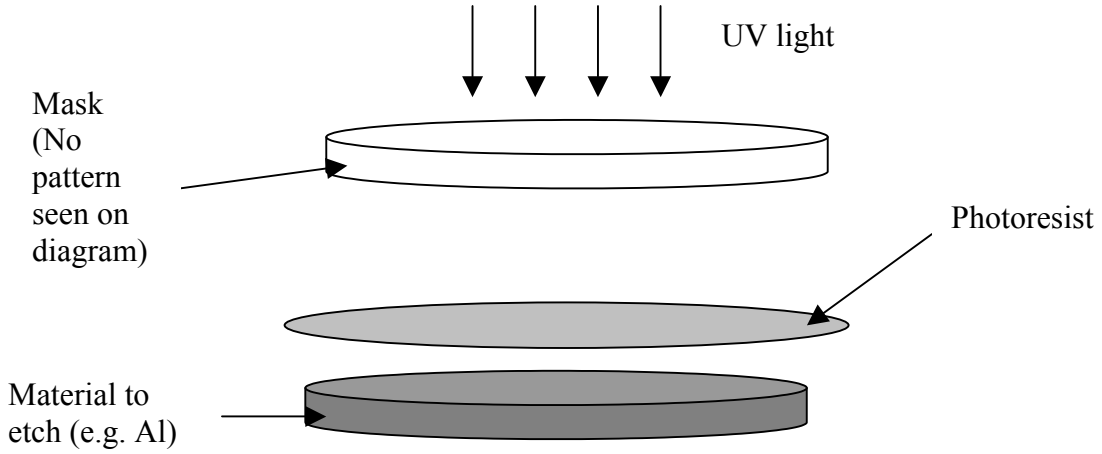

Figure 5. Photolithography setup.

Either negative or positive photoresist can be used. Positive photoresist is developed when it is exposed to UV light. Negative photoresist, on the other hand, is developed when it is not exposed to UV light. Hence, negative photoresist is usually used with a clear field mask and positive photoresist is usually used with a dark field mask (assuming that one is using the liftoff method which is described in next section).

Another important decision that must be made in photolithography is whether to use liftoff or etching methods. Etching involves the placement of a photoresist on top of the layer to etch. Then the mask is exposed to UV light, and because the mask blocks UV light where the design pattern occurs, the design is replicated on the photoresist. With the use of an appropriate acid, an imprint of the design is placed on the layer. Liftoff, on the other hand, uses sputter deposition to "grow" the design on the wafer. Liftoff is a more delicate procedure and hence is advisable in highly sensitive wafer production. However, etching allows for the addition of thicker layers.

3.2.2 Thermal Oxidation / Sputtering

The actual addition of new layers (layers to be later etched using photolithography) is done through two processes, thermal oxidation and sputtering. Thermal oxidation is most commonly used to grow the initial SiO_2 layer on top of the silicon wafer. Heating the silicon wafer to a very high temperature (usually above 900°C) grows this SiO_2 layer. However, as a result of the chemical reactions that bind the growth of this layer, only a relatively small amount can be added (approximately 500 nm). To add larger amounts of SiO_2 or any other type of layer (e.g., Al or Au layer) requires using the process known as sputter deposition. Sputter deposition excites an element (such as Al or Au) to a point that it vaporizes and then condenses on top of the silicon wafer. This creates a uniform layer of that element on top of the wafer However, sputter deposition, although allowing for greater thickness, is not as accurate as thermal oxidation.

3.2.3 Experimental Wafer Fabrication

To fabricate the specific wafer used for experimentation, the following methods were employed. A 2-inch silicon wafer was used for fabrication. The first layer added was an electrically insulating 500 nm SiO_2 layer. This layer was grown using thermal oxidation at a temperature of 950°C. The SiO_2 prevented the electrical properties of the silicon wafer from playing a role in the circuit.

The next layer added was a combination of a Cr and Au layer. First, a 10 nm Cr layer was sputtered on top of the SiO_2. Next, a 190 nm Au layer was sputtered on top of the Cr layer. Au has superior conductive properties, making it an excellent element for the first layer in the design. But Au easily peels off SiO_2. Since Cr has adhesive properties it was added to enable the Au layer to be more easily attached to the silicon wafer. After standard photolithography procedures were performed (clear field mask, 1.2 μm negative photoresist with liftoff method), the first layer of the AutoCAD model was imprinted on the Au layer.

After photolithography, an additional 150 nm SiO_2 layer was deposited on top. Unlike the first SiO_2 layer, this layer was deposited using sputtering. Layer 2 in the AutoCAD design (the layer that etches out contact points between the now "buried" first layer and an outside AC signal source) was imprinted on this SiO_2 layer using a clear field mask, positive photoresist, and the etching method of photolithography.

Next, the passive electrode layer (layer 3 in the AutoCAD model) was added by using again the liftoff method with clear field masks and a negative photoresist. This layer was made of a 100 nm Ni-Cr alloy, chosen for its Young's Modulus. This design required a material of high Young's Modulus so that it would not easily bend when a nanowire assembled on top of it. Although Cr would have been a more optimum layer, a Ni-Cr alloy was used instead because of constraints in the University of Pennsylvania's Microfabrication Facility.

The last layer added, specifically for the "clamped" version, was an additional 100 nm Ni-Cr alloy. Using liftoff with clear field masks and a negative photoresist, the fourth layer was added after electrofluidic assembly had occurred.

3.3 Assembly Parameters

Three properties decide whether a nanowire will assemble during electrofluidic assembly. These three properties are the voltage, frequency, and time for the applied electric field. The importance of each parameter is described below.

The peak-to-peak voltage is important for the AC signal source because a stronger electric field will have a greater chance to cause assembly. Although it may seem logical to consequently increase the magnitude of the voltage to the highest extent, maximizing the voltage has adverse effects because the passive electrodes may burn out. If too strong an electric field is induced across these passive electrodes, the capacitor-like electrodes,

will burn out (similar to a capacitor burning out when exposed to a very strong electric field). As with a capacitor, the larger the spacing between the two pairs of passive electrodes, the stronger the electric field required to burn them out. Hence, a 30 μm gap has a very small chance of a burnout compared to a 5 μm gap.

The second parameter deciding nanowire assembly yields is AC signal source frequency. AC fields allow for the polarization of nanowires so that they can properly assemble across the passive electrodes. A higher frequency will cause a faster polarization of the nanowires, and consequently, faster assembly. However, too high a frequency causes no polarization. In this case, the shifting electrical signals change too quickly for the nanowires to polarize. Hence, they stay as they were, in a nonpolarized state. Optimum frequency is heavily dependent on the types of nanowires used.

The last parameter that decides nanowire assembly yields is the length of time the AC signal source is applied. As with voltage, long time periods usually have adverse effects, such as causing greater electrode burnouts.

3.4 Assembly Setup

An alternating electric field is applied between arrays of adjacent 10-μm-wide metal electrodes separated by 60 μm. The field is obtained by applying a 100 kHz signal from a Topward 8110 function generator between a second pair of electrodes isolated from the top alignment electrodes by 500 nm of SiO_2. This signal is then amplified by a Bogen GA-6A amplifier and applied to the electrodes through an Electroglas Wafer Prober 131.

The optimal conditions for assembling Rh nanowires were applying an alternating field of 100 kHz – 10 V_{pp} for 5 minutes. The optimal conditions for assembling MWNTs were applying an alternating field of 100 kHz – 45 V_{pp}, also for 5 minutes. The optimal conditions for assembling GaAs nanowires were applying an alternating field of 100 kHz – 10 V_{pp} for 1 minute. Furthermore, the GaAs nanowires needed to be sonicated for 5 minutes prior to assembly. Without this sonication, the nanowires tended to clump together, making it difficult to isolate a single nanowire for testing.

An important factor of the assembly was the ability to reuse chips for multiple trials. Chips were cleaned by be being covered in acetone and sonicated for 5-10 minutes. The chips were observed during sonication to ensure that the top layer of electrodes was not being removed.

3.5 Electrical Characterization Setup

Electrical characterization was performed on Rh rods and MWNTs. Unfortunately, the dimensions of the GaAs nanowires made it impossible to run electrical tests on them. The length of these nanowires was approximately 2 μm, so they had to be assembled on chips with gap sizes of 2 μm or less. The chips used were fabricated 2 years ago without allowing for the capability to test nanowires electrically. A solution to

this problem was to design a final mask to act as the top layer, allowing electrical measurements of the assembled GaAs wires. Unfortunately, the drawings used to fabricate these chips did not include alignment marks. Thus, aligning this final layer would have been very difficult.

A final mask layer was designed and fabricated to make electrical measurements possible, but, unfortunately, it was not used for actual testing. There are plans for the mask and chips to be sent elsewhere to do electrical testing.

Electrical characterization of Rh rods and MWNTs was performed in ambient atmosphere. I-V relationships were measured at changing temperatures to calculate a trend in resistance. The devices were probed using a Micromanipulator 6000 probe station along with a Bausch & Lomb MicroZoom II microscope. A Hewlett Packard 4145B Semiconductor Parameter Analyzer was used to measure and record the I-V characteristic. The temperature of the device was raised using a Powerstat Variable Autotransformer (type 3PN116B), which heated up the metal platform on which the wafer rested. The I-V characteristic was then transferred from the Parameter Analyzer to a diskette via a program written for MS-DOS.

4. RESULTS AND DISCUSSION

4.1 "Clamping" Wafer Design

After electrofluidic assembly occurred on these fabricated wafers, the following observations were made. First, the optimum parameters for assembly for the "clamped" version were at 30 volts peak to peak at 100 kHz for 300 seconds. Second, the "unclamped" version had greater resistance to assembly than did the "clamped" version. This can be attributed to the "unclamped" version's extra capacitive properties. The "unclamped" version had two 200-μm-square contact pads in addition to the passive electrodes. These relatively large square pads probably caused greater capacitive properties to be exhibited by the assembly sites. To alleviate this property, it is advised that higher peak-to-peak voltages be introduced. Third, increases in time usually had a diminishing return after a certain point. After about 300 seconds, any increase in time had little effect in gaining higher yields for this circuit. In fact, increasing times to 600 seconds actually caused more electrode burnouts than it did additional nanowire assembly. Fourth, nanowire assembly was most likely between the gaps that had similar lengths as the nanowires. Finally, all nanowire assembly at gaps above 20 um was extremely unstable and easily breakable.

Only a quarter of the wafer design described in section 3.1.1 was used. This quarter wafer included four "clamped" version circuits with a total of 400 possible assembly sites (see Figure 6). After clamping occurred, the wafer was cut into four pieces with one circuit per new chip. Results of nanowire assembly yields after clamping are shown in Table 1. Furthermore, voltage, frequency, and time parameters are displayed below Table 1 as well as their effects.

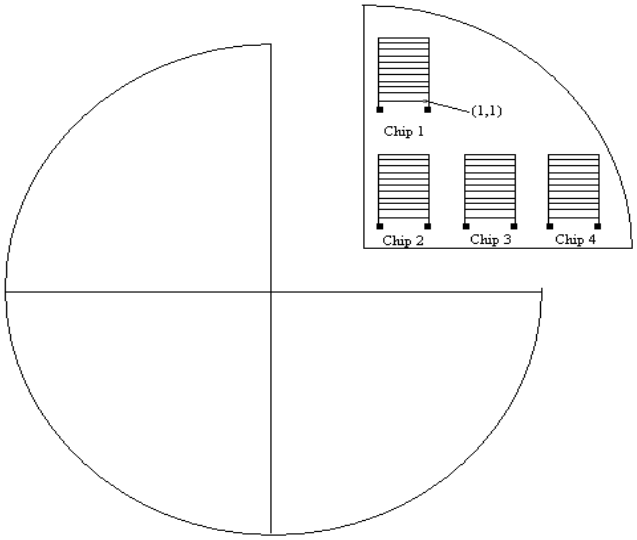

Figure 6. Chip location and details (figures not drawn to scale).

Chip 1	**Chip 2**	**Chip 3**	**Chip 4**
(1,2) (1,4) (1,7) (1,8) (2,5) (2,6) (2,7) (2,8) (3,1) (3,7) (4,5) (4,8) (4,9) (7,3)	(2,1) (2,6) (3,10) (3,8) (3,6) (3,5) (3,4) (7,10)	(1,9)	None

Table 1. Nanowires successfully "clamped"

Note: (1,2) and (1,8) had 2 and 3 nanowires, respectively, for Chip 1. (3,5) and (3,6) had 2 nanowires each for Chip 2. Parameters for assembly are 30 volts, 100 kHz for 300 seconds.

After the fourth or "clamping" layer had been placed, the chip was cut to create four pieces, each containing a circuit (see Figure 7). All nanowires that successfully clamped (as indicated in the table) remained clamped.

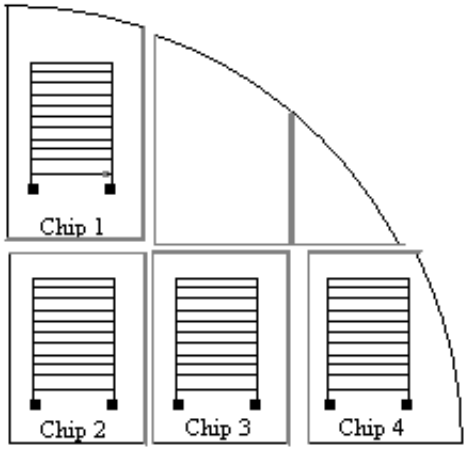

Figure 7. How the chips were cut.

The following are two pictures taken with a Scanning Electron Microscope (SEM) of the assembled nanowires for Chip 2:

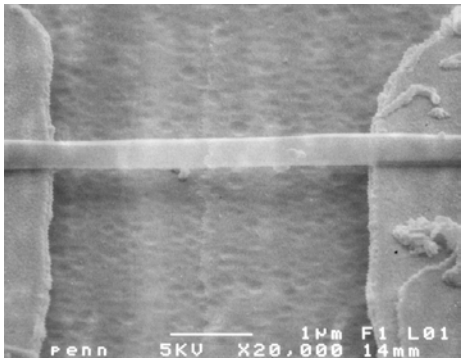

Figure 8. SEM of (2,6) on Chip 2.

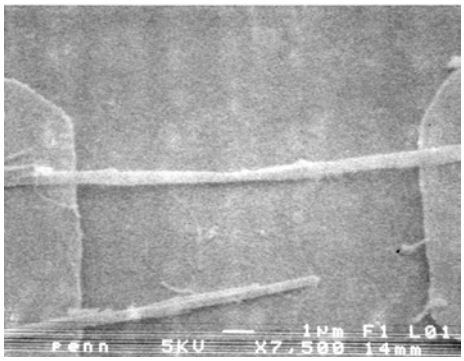

Figure 9. SEM of (7,10) on Chip 2.

4.2 GaAs Nanowires

GaAs nanowires were successfully assembled on chips with gap sizes of 1-3 µm. Figure 10 shows a picture taken with a SEM of a particular GaAs nanowire. Electrical testing could not be completed because of limitations of the chip. A final mask layer, however, was designed and fabricated to enable electrical testing. The lack of alignment marks on the original drawings will make this final layer difficult, although not impossible, to align.

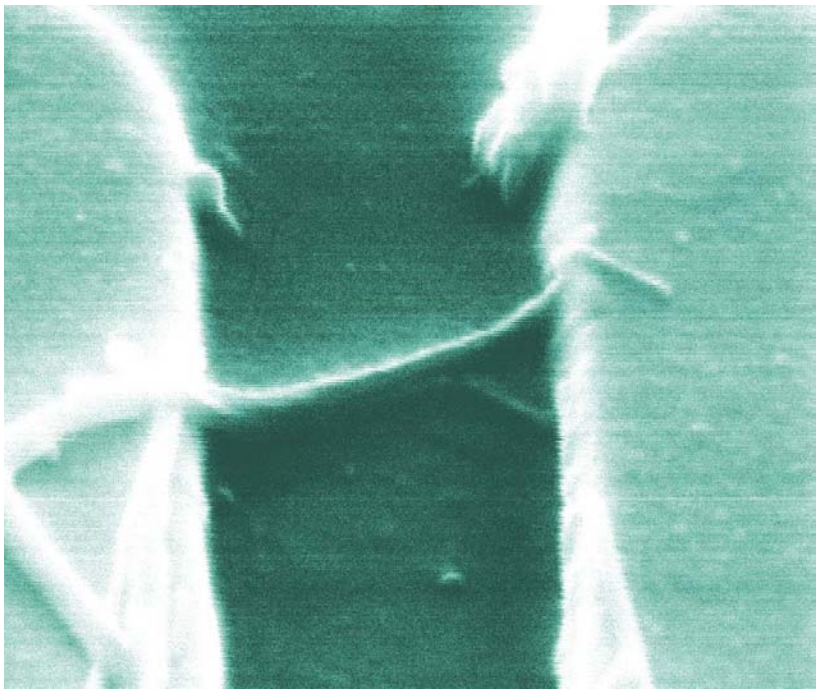

Figure 10. A picture of a GaAs nanowire taken with a SEM.

To overcome the problem of the lack of alignment marks, pre-existing features on the chip were used as alignment marks — specifically, the electrodes at sites (1,9) and (9,9). Their functionality will be sacrificed, however, because they will be exposed to UV light and thus destroyed. This was a tradeoff in designing the final layer.

A possible problem in making electrical measurements may be the large resistance of the GaAs nanowires. The resistivity of undoped GaAs at room temperature is 10^7 Ω·cm. The length of the wires is approximately 2 μm, and the wires are 20-80 nm in diameter. Assuming a diameter of 50 nm, this yields a cross-sectional area of 7.85e-11 cm^2. Using the equation $R = (\rho l)/A$, the resistance can be calculated to be 2.5e13 Ω. This is an extremely large, though expected, value for resistance. GaAs is a semiconductor, so the resistivity is expected to be higher than that of conductors. Furthermore, the wires are so thin that the ratio of l/A is quite large. Such a large resistance will complicate electrical measurements because large values are difficult to sense accurately. Methods of lowering the resistance include doping the wires or raising the temperature. Since GaAs is a semiconductor, both of these methods will decrease the resistance, thus making resistance a characteristic that can be measured by available instruments.

4.3 Rhodium Nanowires

Rh nanowires were successfully assembled on various chip designs. They were first successfully assembled on chips with a gap size of 1-3 μm. The optimal conditions for these chips were a signal at 100 kHz – 15 V_{pp} for 5 minutes. These wires could not be tested because of the limitations of the chips. A successfully assembled Rh nanowire on these chips is shown in Figure 11.

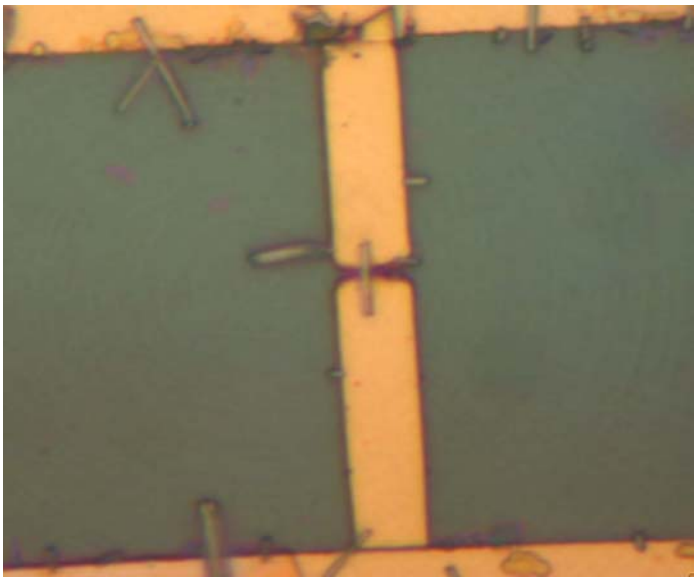

Figure 11. An assembled Rh nanowire.

The Rh nanowires were also successfully assembled on chips with gap sizes of 5-30 μm. Since the gap sizes are larger on these chips, a stronger field must be applied to the chips to achieve successful assembly. Thus, the optimal conditions for these chips were a signal at 100 kHz – 40 V_{pp} for 5 minutes. This stronger field did not damage the chips at all because the spacing of the features was relatively large.

Testing of the Rh nanowires was done on the second group of chips (with gap size of 5-30 μm). Figure 12 shows the I-V characteristic for a Rh nanowire at room temperature. The slope of this line is 0.0036 A/V, which yields a resistance of 277 Ω. The resistivity of Rh is known to be 4.3 μΩcm. The nanowire was bridging a gap of 5 μm, so the length will be assumed to be 5 μm. The diameter of the nanowires is approximately 200 nm, which yields a cross-sectional area of 3.14e-10 cm^2. These values give a theoretical resistance of 6.85 Ω. This indicates that the measured resistance values include a large contact resistance between the Rh rod and the Ni-Cr electrode on which it rested.

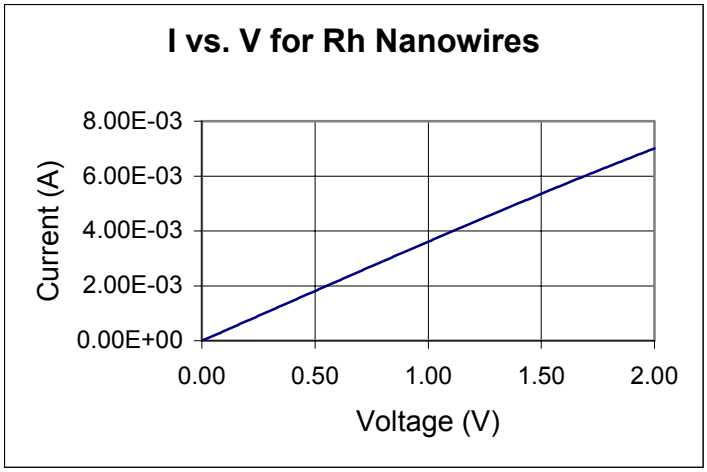

Figure 12. I-V characteristic for a Rh nanowire

The temperature was then raised to measure the I-V characteristic again. Unfortunately, once the temperature reached 50ºC, the I-V characteristic became noise. Inspection with an optical microscope showed that the Rh rod had burned at the end and had become disconnected from the electrode. A method of preventing this in the future may be to increase the temperature more slowly. Rapid changes in temperature may have been too strenuous on the materials used. Thus, slowing down the change in temperature may prevent the rod from burning and allow accurate data to be taken. This method was not implemented in this project because of both time and equipment constraints.

4.4 Multi-walled Nanotubes

Multi-walled carbon nanotubes (MWNTs), while more difficult to assemble than Rh nanowires, proved to be more easily measured while raising the temperature. Figure 13 shows the I-V characteristics for MWNTs at different temperatures. From these data, it is evident that as the temperature increases from room temperature to 125°C, the resistance of the MWNT decreases. At room temperature, this particular MWNT had a resistance of approximately 200 kΩ. At 125°C, the same MWNT had a resistance of approximately 100 kΩ.

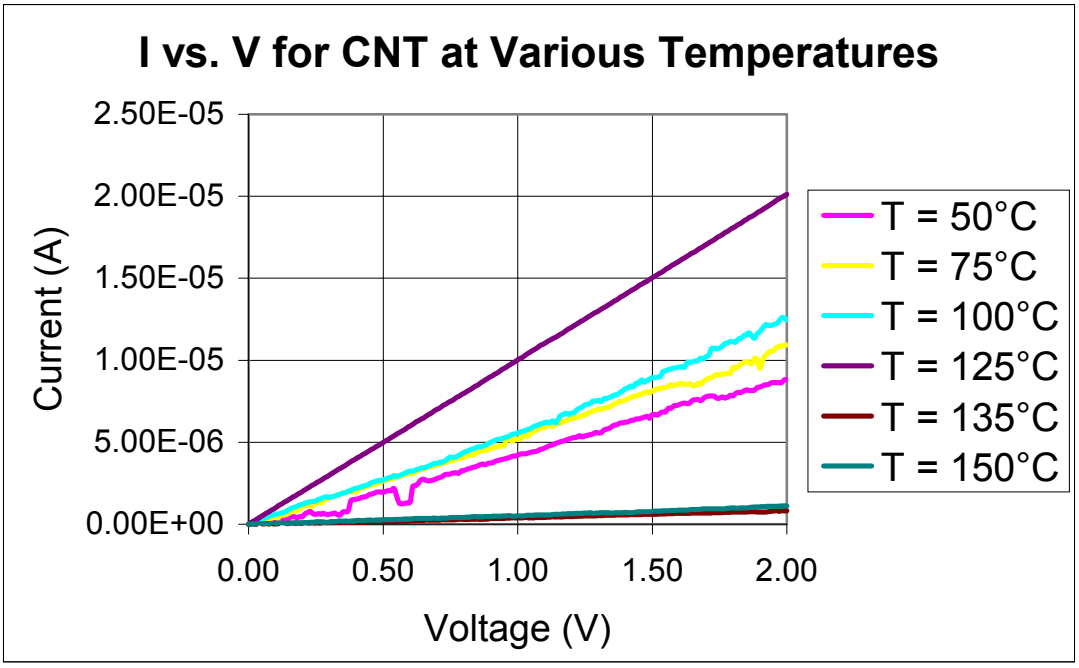

Figure 13: I-V characteristic for an MWNT at different temperatures.

These data are not unexpected. The MWNTs used are essentially sheets of a graphite lattice rolled into a cylinder. The MWNTs can be thought of as objects in three dimensions: *a*, *b*, and *c* (see Figure 14). The *a* and *b* dimensions represent the horizontal plane of the lattice, while the *c* direction represents the vertical plane. Electrically, graphite is a semi-metal, which means that it is a conductor in the *ab* plane and an insulator in the *c* plane. When conductors are exposed to heat, their resistivity will increase. When insulators are exposed to heat, their resistivity will decrease.

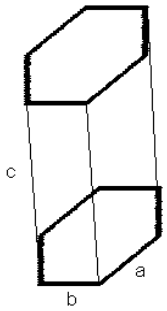

Figure 14. A structural representation of graphite.

The MWNTs were fabricated such that resistance was being measured across the insulating *c* plane. Resistivity is known to decrease with temperature along this plane, so decreasing resistance is normal.

The data in Figure 13 were then used to calculate an energy barrier that is common to semiconductors. For any wire, $R = (\rho l)/A$ or $R = l/(\sigma A)$, where ρ is the resistivity and σ is the conductivity. Furthermore, $\sigma = n\mu q$, where n is the carrier concentration, μ is the mobility of carriers, and q is the charge of an electron. Thus, it

follows that R = l/(nμqA). For semiconductors at high temperatures, resistance is dominated by the carrier concentration n. The equation relating carrier concentration and temperature is $n = (N_c N_v)^{1/2} e^{-E/(kT)}$, where n is the carrier concentration and E is the energy barrier. If ln(n) vs. 1/T is graphed, then the slope of that graph is equal to –E/k. Ln(n) vs. 1/T was graphed for this MWNT, and the slope was calculated to be $-1482\ K^{-1}$. This graph is seen in Figure 15. By using the fact that $-1482\ K^{-1} = -E/k$ where k is the Boltzmann constant, it is shown that E = 2.05e-20 J, or E = 0.13 eV.

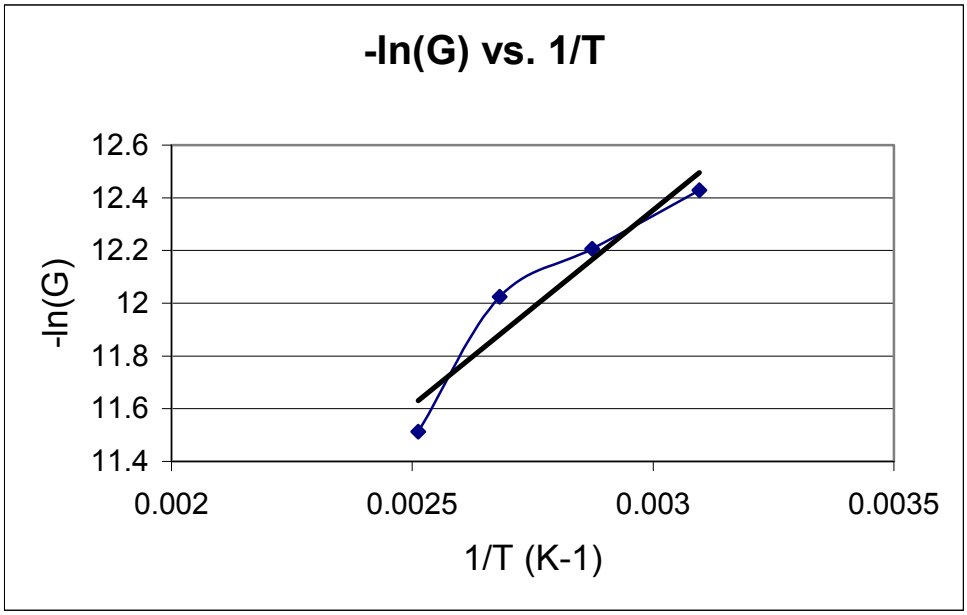

Figure 15. –Ln(G) vs. 1/T for an MWNT. This graph was used to calculate the energy barrier.

This value is quite small when compared with band gaps of semiconductors, because the MWNTs are not semiconductors. Their decrease in resistance with respect to temperature may not be due mostly to carrier concentration. On the contrary, the increasing temperature may be affecting the mobility of the charges, rather than their concentration. In that case, the above equations should be ignored.

Using the equation R = ρl/A, the theoretical resistance of these nanotubes can be calculated. The resistivity of the nanotubes is given as 55 μΩ cm. The nanotube was bridging a gap of 15 μm, so the length of the tube is approximated to 15 μm. The outer diameter of the nanotubes was estimated using a picture taken with a SEM. It was approximated to be 600 nm. The walls of the tubes were given as 12 nm, which yields an area of approximately 2.22e-10 cm^2. These values yield a theoretical resistance of 372 Ω.

The slopes on the graph of Figure 13 can also be used to calculate the resistance of the nanotubes. The slopes of the graph are equal to 1/R, where R is the resistance of the MWNT. At room temperature, the slope was approximately 5e-6 A/V, which gives a resistance of 200 kΩ. This value is three orders of magnitude larger than the theoretical resistance calculated in the previous paragraph. Therefore the measurements were

including a large contact resistance between the MWNT and the Ni-Cr electrode on which it rested.

Furthermore, data were taken on MWNTs that bridged gaps of varying sizes. At room temperature, a nanotube that was 10 μm long demonstrated a resistance of 33 kΩ. This finding is consistent with the fact that as the length decreases (from 15 μm to 10 μm) the resistance should also decrease. However, at room temperature, a nanotube that was 6 μm long demonstrated a resistance of 310 kΩ. Since this nanotube was shorter, it should have yielded a resistance that was smaller than the previous two nanotubes. The fact that it did not also supports the idea that the resistance measurements were including a large contact resistance.

However, the data presented here can still be used to assert the fact that resistance will decrease with an increase in temperature. The contact resistance between the nanotube and the electrode remained constant throughout the tests, as the nanotube did not move. Thus, the resistance values measured may not be the actual resistance of the tubes, but they will all differ from the actual value by the same constant. The trend of decreasing resistance is still valid.

The trend of decreasing resistance, however, does not continue with an increase in temperature. Between 125°C and 135°C, the I-V characteristic changes drastically. Between these two temperatures, the resistance of the MWNT increased from 100 kΩ to 2 MΩ. This trend of decreasing resistance and then increasing resistance was repeated in other trials. A possible explanation is that between 125°C and 135°C a critical temperature was reached that fundamentally changes the electrical properties of the tubes.

The resistance trend was then measured in the reverse direction to see if, after raising the temperature and lowering the resistance, lowering the temperature could result in an increase in resistance. Since in previous tests the data indicated a critical point between 125°C and 135°C, the temperature was raised only to 100°C. Figure 16 shows the data taken when the temperature was raised and then lowered. A (D) next to the temperature in the legend indicates that the temperature was raised and then lowered back down to the recorded temperature. Again, as expected, the current increased with an increase in temperature. This shows a decrease in resistance with an increase in temperature.

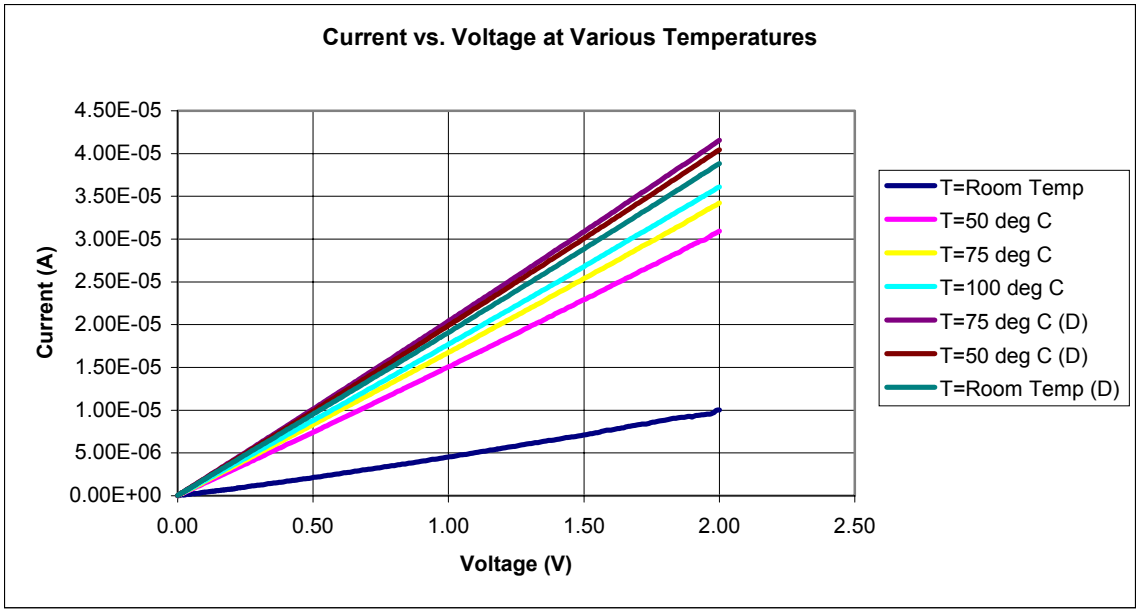

Figure 16. I-V characteristic for an MWNT at various temperatures.

When the heater was turned off and the temperature was lowered, however, the resistance did not increase again back to its original value. Instead, the resistance remained at the value it had reached at 100°C. The data indicate that the resistance may have even decreased a bit more after the heater was turned off.

There are various possible explanations. One explanation is that the temperature being measured was the temperature of the metal surface on which the wafer rested. The thermometer was resting on the same metal surface as the wafer, thus measuring the temperature of the surface. The temperature of the electrodes and the nanotube may have been different. The Ni-Cr electrodes may have taken longer to cool down than the metal surface. This explanation is supported by the data demonstrating that the resistance decreased a bit even after the heat was turned off. This shows that the electrodes and nanotube on the chip were slow to react to the change in external temperature. Thus, when the external temperature had cooled to 50°C, the temperature of the nanotube may still have been at 100°C. Also, data taken after the heat was turned off indicate a small increase in resistance. This suggests that the resistance is actually increasing, but it is unclear if the resistance value will return to the original room temperature value.

Another possible explanation is that heating the nanotube permanently changes the electrical properties of the tube. Hence, once the temperature is raised and the resistance is decreased, the resistance will never increase again. Resistance values were not coming down as quickly as they should have been once the heat was turned off. While the data did appear to be decreasing a bit, the changes in current could have been general fluctuations in measurement, errors caused by the tools that were used. The resistance value may not have been increasing, but rather fluctuating around a certain point. Unfortunately, not enough data were taken at the time to confirm this.

5. CONCLUSIONS

This report demonstrated the assembly parameters and wafer design that enabled electrical characterization of various types of nanostructures. It showed that large electrode pads on the Si wafer contributed large capacitive forces that made assembly difficult. Thus, when assembling nanowires or nanotubes, it is preferable to assemble on a chip without these large pads. However, for testing, these pads are necessary to probe from the outside world. One way to overcome these capacitive forces was demonstrated in this report. The solution was to assemble nanotubes or nanowires on wafers without these large pads and then do a final layer of processing in which they are added through photolithography and metal deposition. This method allows nanostructures to be assembled relatively easily and tested conveniently.

This report also demonstrated the I-V characteristic for Rh nanowires. This information can then be used to calibrate the nanowire if it is used as a sensor. It could, in effect, be used as a thermometer by measuring the resistance and finding the corresponding temperature. More important, however, were the tests done on the MWNTs, which showed that, in general, as temperature increases, the resistance of the nanotube will decrease. These tests also showed that heating the nanotubes permanently may change their electrical properties, as the trend could not be reversed.

6. RECOMMENDATIONS

Future work includes the characterization of GaAs nanowires. Because of the small size of the nanowires, this needs to be done at facilities that have greater resolution photolithography. Furthermore, mechanical tests can be done on all three structures. Resonant frequencies and quality factors could be found for these nanostructures and then be used to create other sensors. Ultimately, various types of nanowires and nanotubes could be placed in a large array. Since different types of nanowires react differently to different stimuli, this array would be capable of sensing multiple substances simultaneously. These types of sensors have applications in everything from medicine to defense.

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