The ENIAC Accumulator and Cycling Unit on a Field Programmable Gate Array (FPGA)

Emily Rose Blem
Advisor: Prof Jan Van der Spiegel
SUNFEST 2003
The ENIAC

- Electronic Numerical Integrator and Computer (1947) – First general purpose programmable computer by Eckert and Mauchly
- ENIAC-On-A-Chip (1997) – implementation with 0.5 um CMOS process true to original architecture with software interface
Project Goals

- Implement ENIAC on FPGA
- Three accumulators, cycling unit, and constant transmitter
- Make system operate like the original ENIAC, from user’s perspective
- Maintain decimal representation of numbers, pulse train, as many details as possible
ENIAC Layout

- Constant Transmitter
- Input/Output Devices
- Program Controls
- Function Tables
- Multiplier, Divider, Square Rooter
- Accumulators
- 17 meters
- 10 meters
Cycling Unit

• Pulse train: like having 10 different clocks
• Each signal acts as a clock to control specific operations
• Maintained where possible

Pulse train supplied by cycling unit
Representing Numbers

- Decimal Representation
- Ring counter: numbers are incremented by shifting to the right and setting carry flag
- Simulated on FPGA with 10-bit register
- Numbers are transmitted as pulses
Components on FPGA

- Clock Divider
- Control Unit
- Cycling Unit
- Start Up
- RAM
- Receiver
- Sign Unit
- Transmitter
- LED
Input/Output Connections

Switch Select: 4 ops (8), 2 repeats (10), clear correct (4), sig dig (10)

Program Pulse Out

Digit Trunk Input Select

4-16 Decoder

FPGA

Data bus: op, repeat, and sig dig switches have built in encoders, bank of four clear correct switches input at once (each have one choice)

Select Clear Switch

LED out: column (4) and row (4)

Digit Trunk Input

Digit Trunk Inputs from other units

Buffer

Program Pulse In
Implementation

Digilent Digilab II XL Board with Xilinx Spartan II FPGA

Printed circuit board designed by Zheng Yang for testing
Demonstration
Conclusions and Future Work

- Transmit pulses between two accumulators
- Build constant transmitter
- Add IO for full implementation
- Preserving original architecture on modern hardware is cumbersome, but will add to historical relevance

Thank you for your time and enjoy the rest of your summer!