# The ENIAC Accumulator and Cycling Unit on a Field Programmable Gate Array (FPGA)

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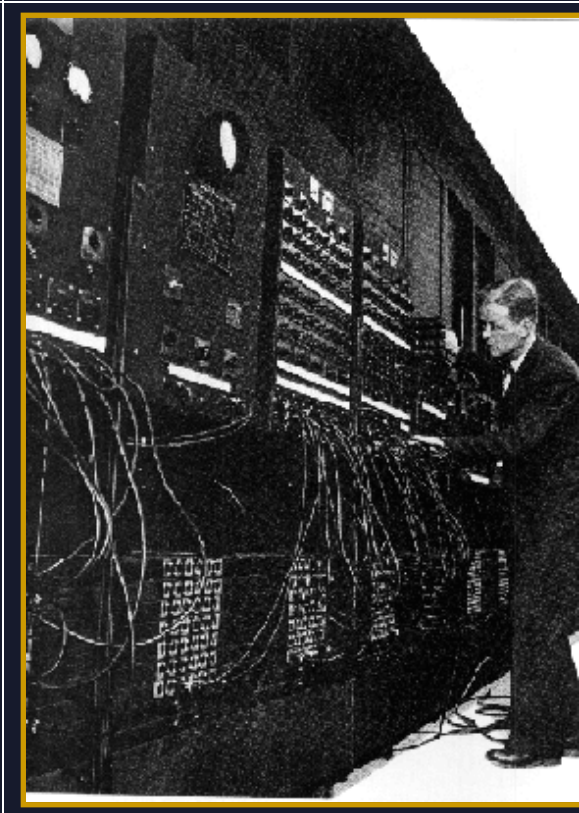


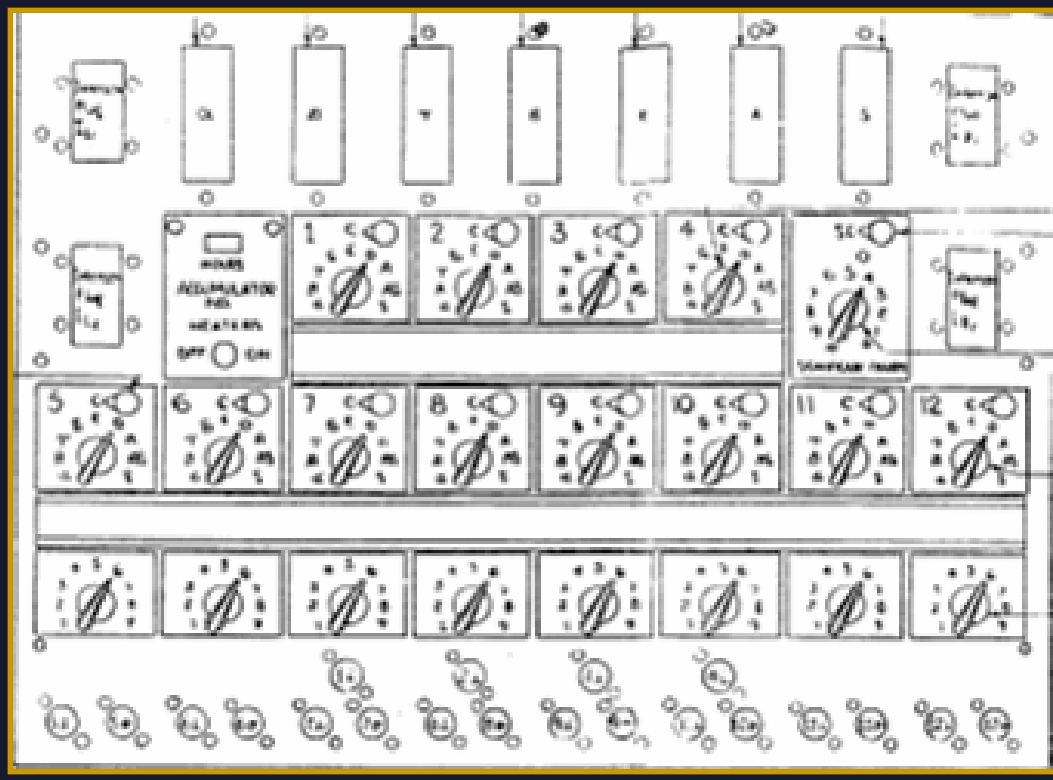
# The ENIAC

- Electronic Numerical Integrator and Computer (1947) – First general purpose programmable computer by Eckert and Mauchly
- ENIAC-On-A-Chip (1997)– implementation with 0.5 um CMOS process true to original architecture with software interface

ENIAC in operation

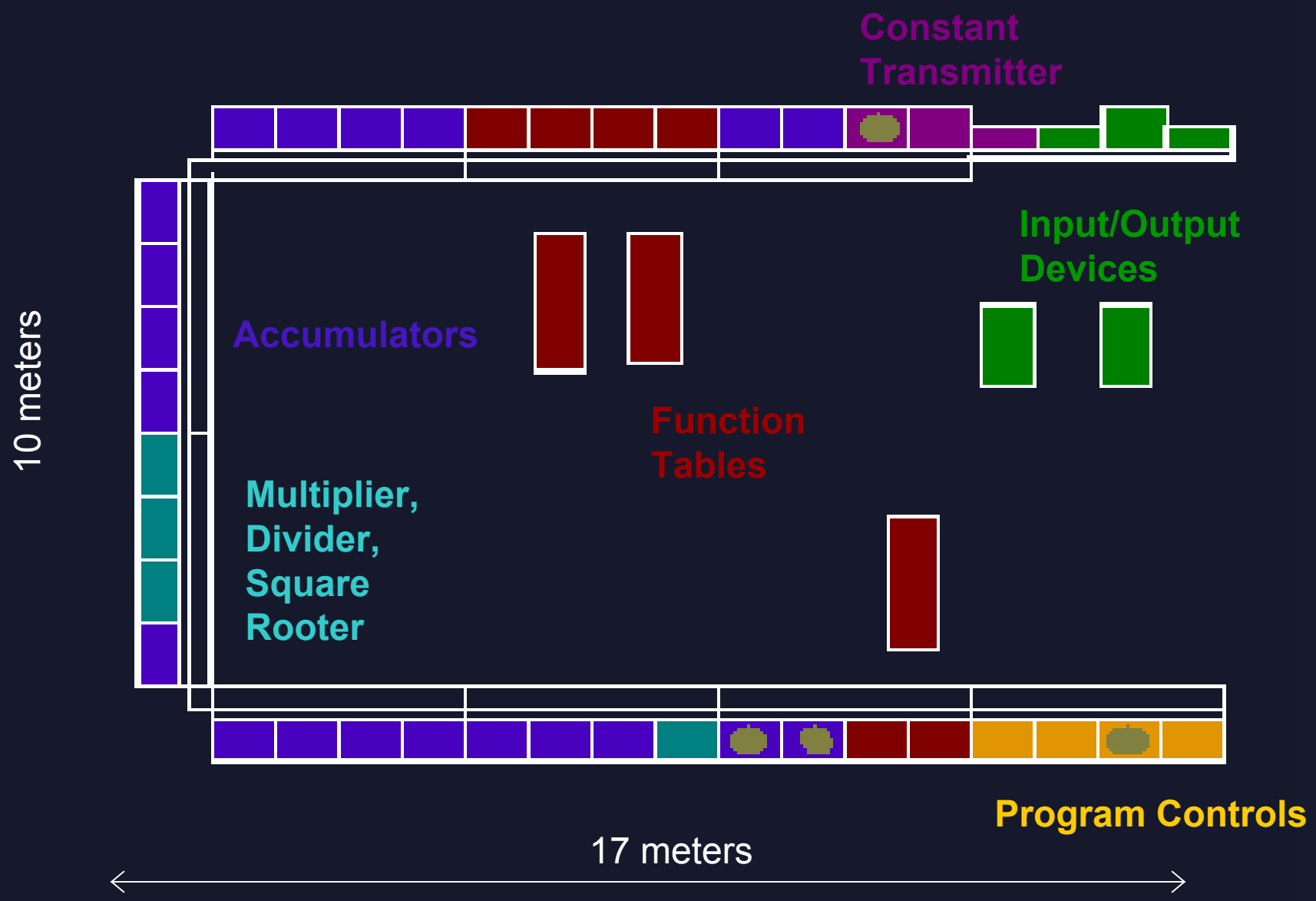
# Project Goals

- Implement ENIAC on FPGA
- Three accumulators, cycling unit, and constant transmitter
- Make system operate like the original ENIAC, from user's perspective
- Maintain decimal representation of numbers, pulse train, as many details as possible



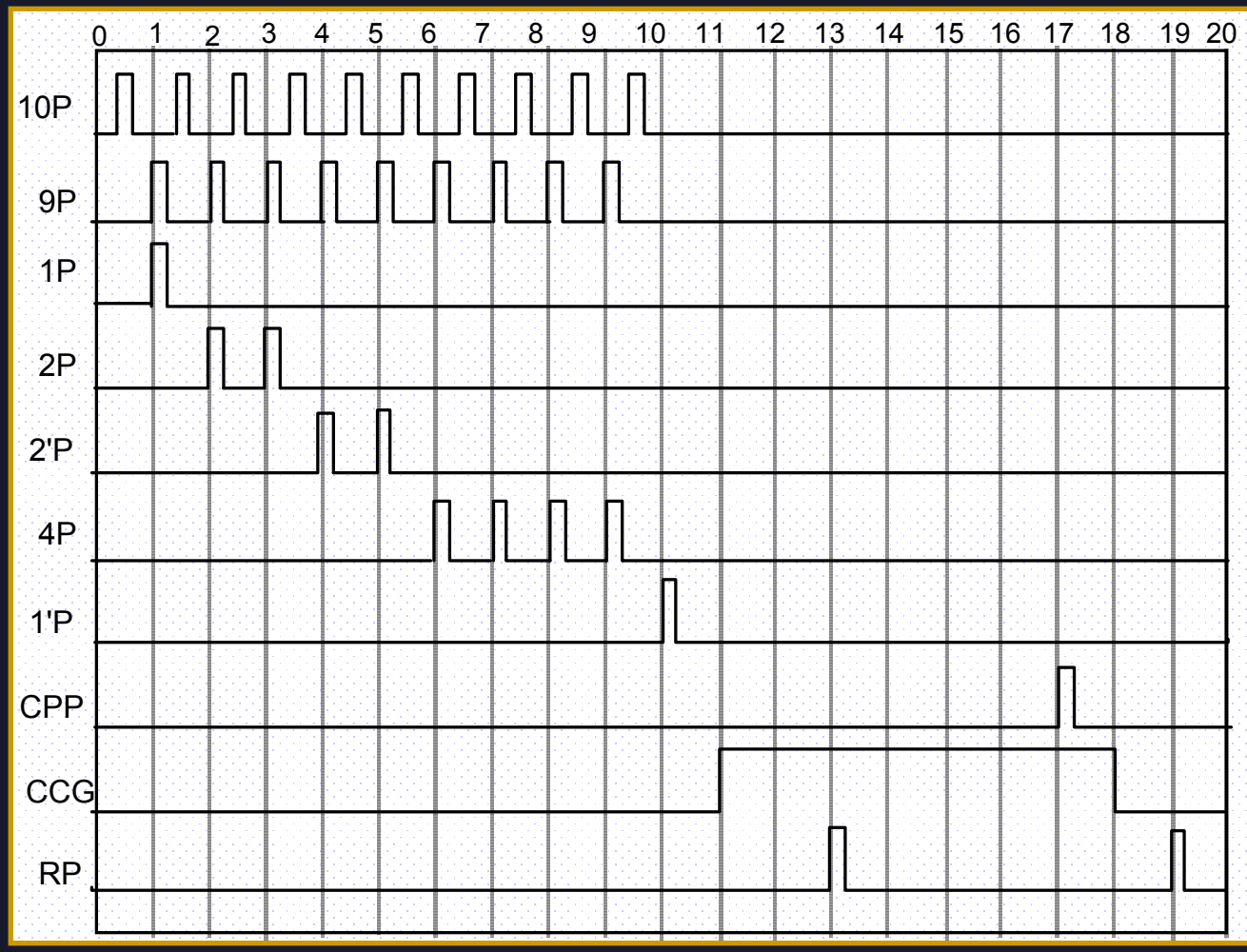
Accumulator Panel

# ENIAC Layout



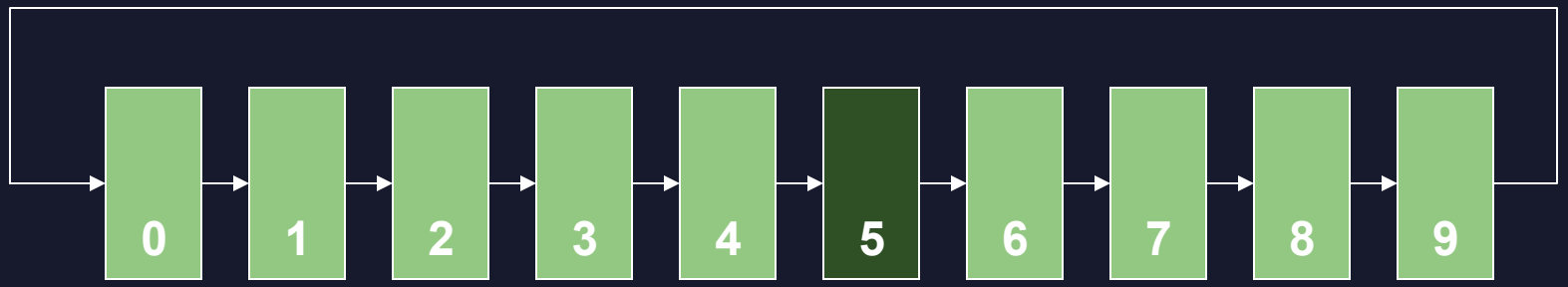
# Cycling Unit

- Pulse train: like having 10 different clocks
- Each signal acts as a clock to control specific operations
- Maintained where possible



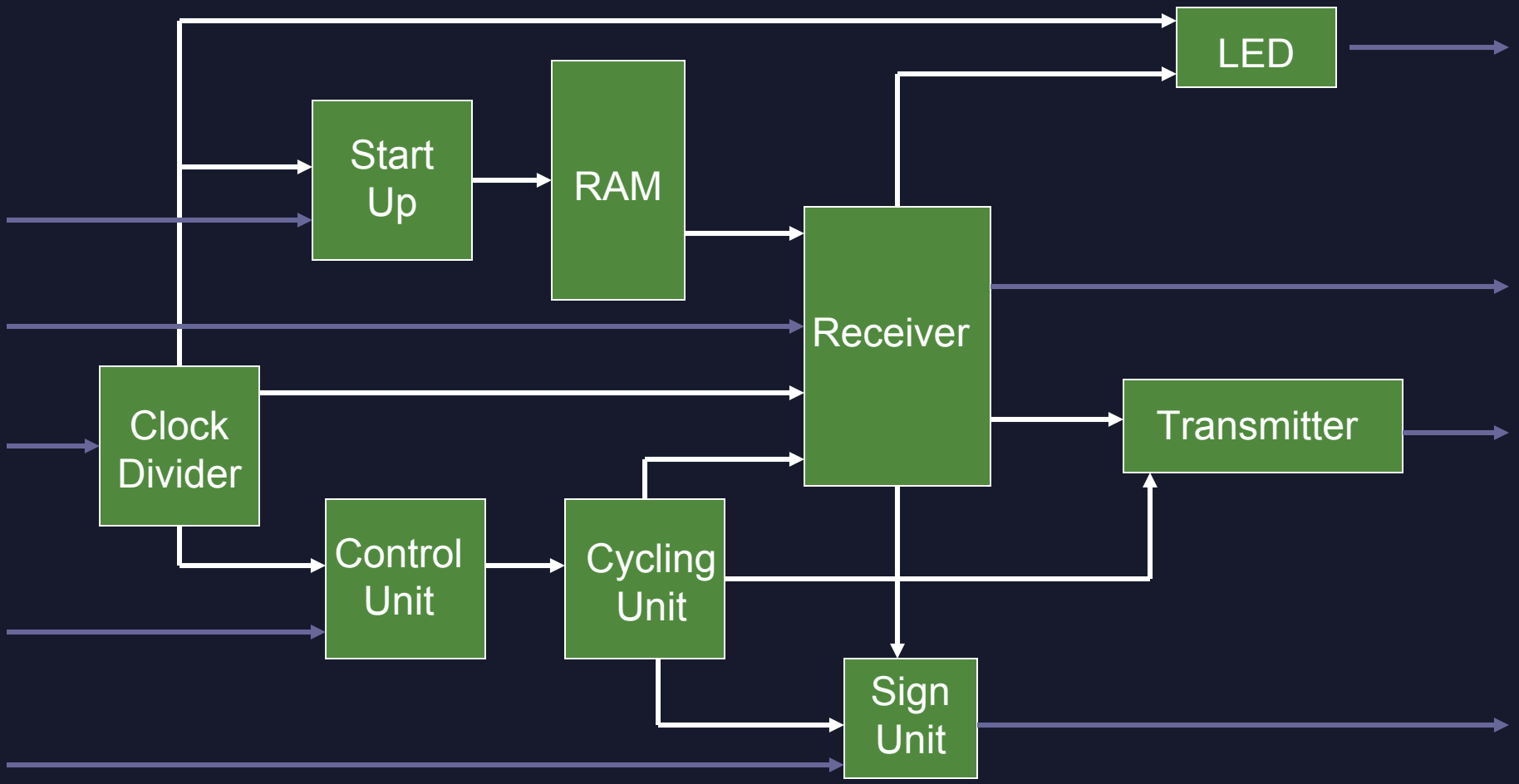

Pulse train supplied by cycling unit

# Representing Numbers

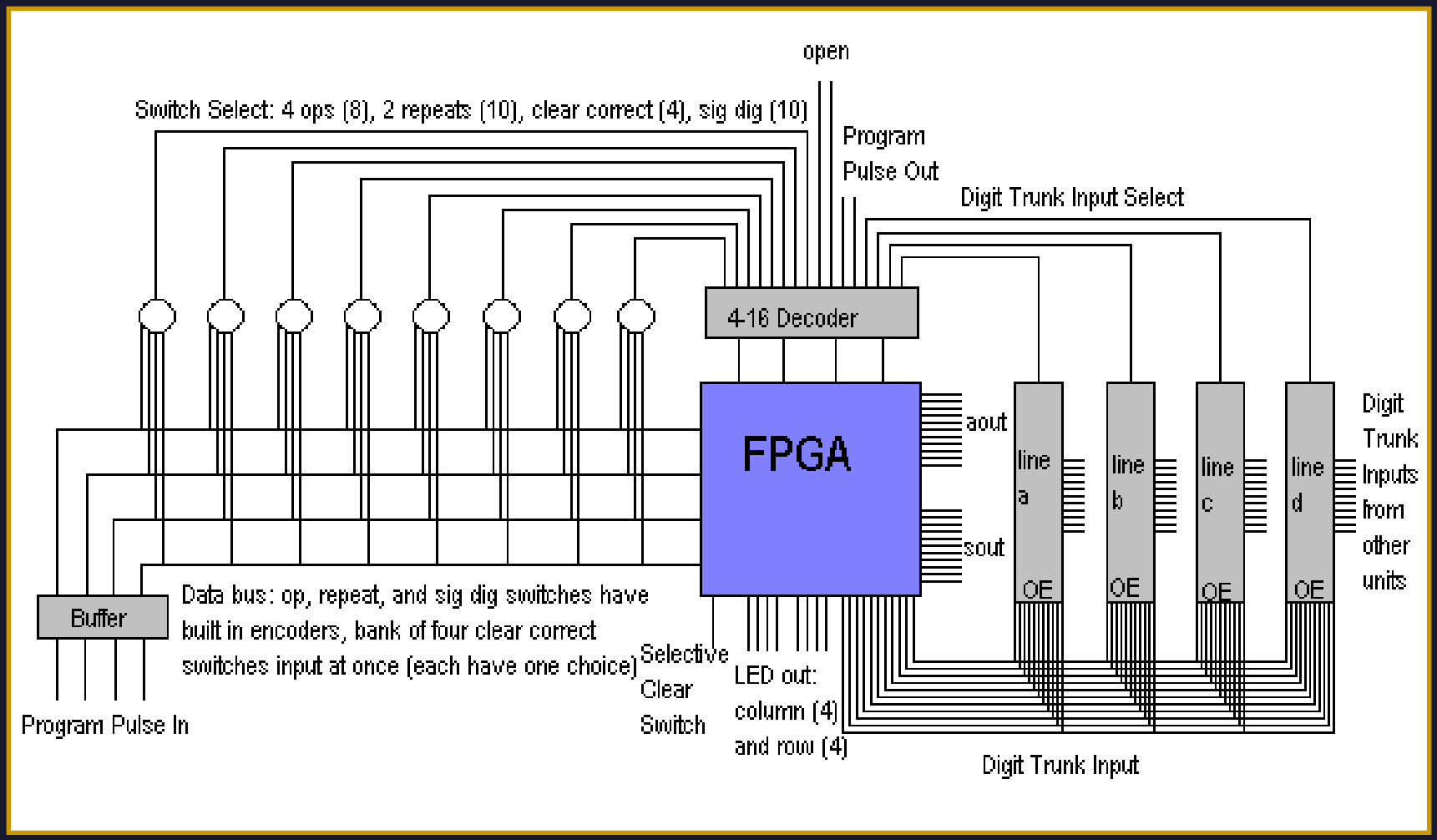



- Decimal Representation
- Ring counter: numbers are incremented by shifting to the right and setting carry flag
- Simulated on FPGA with 10-bit register
- Numbers are transmitted as pulses

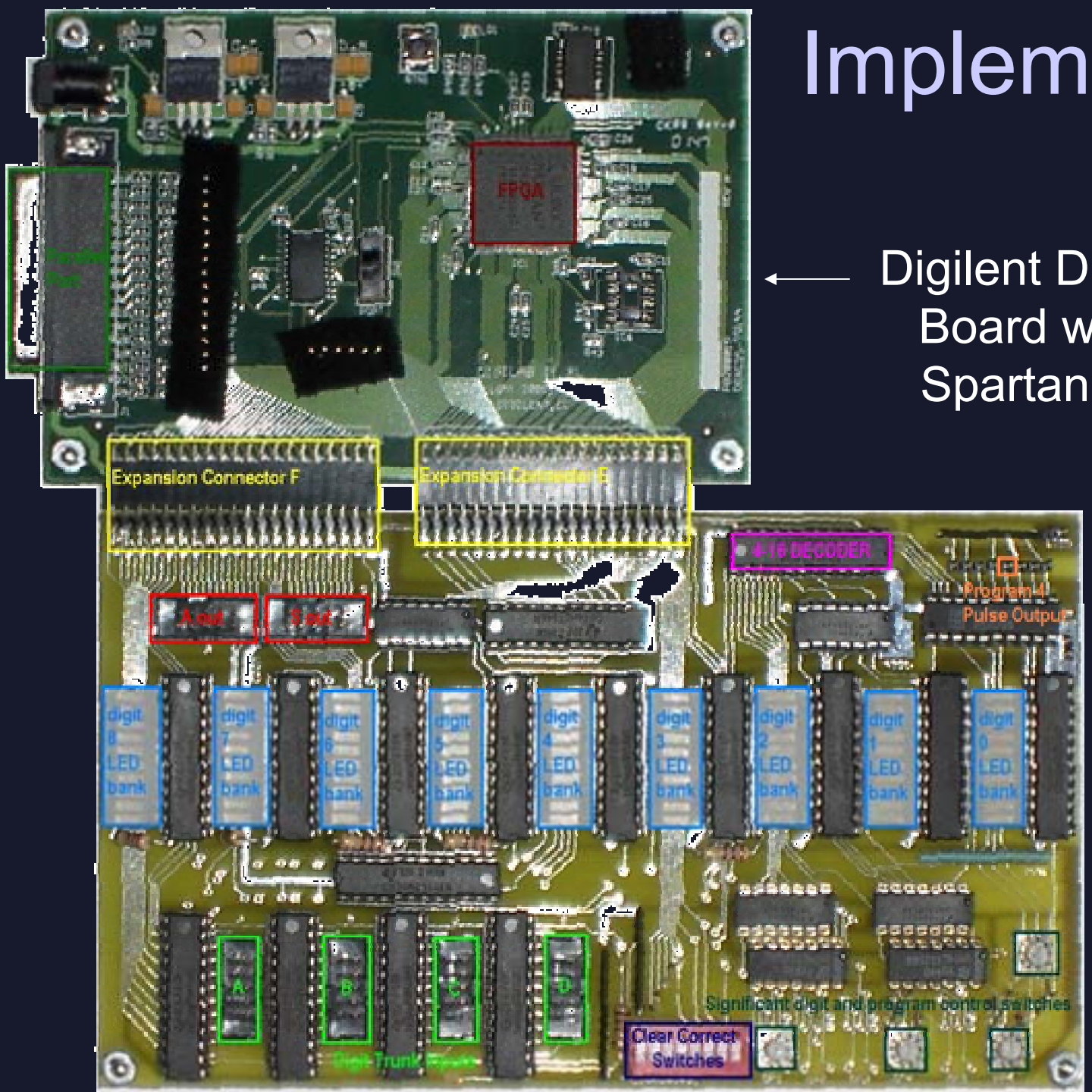
# Components on FPGA



# Input/Output Connections



# Implementation




← Digilent Digilab II XL Board with Xilinx Spartan II FPGA

← Printed circuit board designed by Zheng Yang for testing

# Demonstration

# Conclusions and Future Work

- Transmit pulses between two accumulators
- Build constant transmitter
- Add IO for full implementation
- Preserving original architecture on modern hardware is cumbersome, but will add to historical relevance

Thank you for your time and enjoy the rest of your summer!