COMPONENTS OF A CMOS IMAGER FOR A POLARIZATION-DIFFERENCE CAMERA

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ABSTRACT

The problem of perceiving objects that are suspended in scattering media limits the ability of humans to derive information about their environment. This can be the cause of several important dangers to personal safety, while it can also prevent people from learning about their surroundings. From studying the visual systems of animals that have a better sense of perception in such media, the concept of polarization-difference imaging was born. A system that employs this technique uses the polarization properties of light in novel ways to produce images that detect objects in scattering media and make surface features discernable. Such a system is a polarization-difference camera. A polarization-difference camera can consist of a polarization analyzer, a solid-state imager, and an image display system. The polarization analyzer separates detected light into orthogonally polarized beams. The solid-state imager transduces the light signals into electronic signals and processes the data to produce the polarization-difference output and other necessary operations. The image display system transforms the data so that images can be optimally displayed. This report focuses on the design aspects of the solid-state imager for a polarization-difference camera. The solid-state imager may be constructed with complementary metal-oxide semiconductor (CMOS) devices, currently the most widely used variety of devices in integrated electronic systems. The pixels used in the imager, which employ active transistors, are known as active pixel sensors. A set of several designs of components that may be used in the solid-state imager are described and analyzed. Suggestions for optimization for an integrated design follow.

1. INTRODUCTION

Much knowledge of our environment is derived from our ability to visually perceive the objects that surround us. Human vision is characterized by the spatial mapping of the intensities of various light frequencies. It allows us to appreciate and decipher the surface features of an object. Of course, this occurs when the object is placed in a medium that does not significantly distort the light travelling from it to our eyes. When we attempt to perceive objects in scattering media, our visual abilities begin to fail us. If light is heavily scattered, as, for example, when one encounters a dense layer of fog, smoke, or a murky underwater environment, objects of appreciable size that lie in close proximity may become difficult to detect or may not be visible at all.

Part of the problem arises from the reflection of background light into the path of light from the object that our eyes are targeting. The tiny particles in a scattering medium

cause the reflection of the background light, called veiling light, which subsequently diminishes our ability to see the light from the object, called image-forming light [1]. This problem is exacerbated when the intensity of the background light is significantly greater than the intensity of the image-forming light, in which case surface features of an object may be hidden even when the degree of light scattering is relatively small. Indeed, our eyes alone may not be able to faithfully target objects and distinguish important surface features in media characterized by heavy scattering.

1.1.1 Biological Basis

Certain animals are known to possess the ability to perceive objects in scattering media more reliably than humans. The green sunfish, for example, can perceive objects in underwater environments that are clouded by plankton and other scattering particles [2]. By studying the visual systems of such animals, researchers hope to construct sophisticated imaging systems that may enable humans to enhance their ability to perceive objects in such environments. The concept of the polarization-difference imaging (PDI) camera is a product of this type of research.

1.1.2 Objectives of the Polarization-difference Camera

The objective of the polarization-difference camera that is the subject of this report is to create reliable imagery of objects in scattering media. The camera should be able to receive an image of a target whose features are clouded by veiling light in a scattering medium and are difficult to distinguish due to high contrasting background light. The camera should then produce an image that amplifies the surface features of the object, without further amplifying background light. We wish to design the camera using integrated microelectronics that can be fabricated on a single microchip. The chip should have the tools to process image data and send out signal results digitally for further processing by external imagery systems. Integrating these tools on a chip may allow the camera to be portable, lightweight, and operable at high speeds [4]. Ultimately, we desire the camera to be able to produce images in real time so that it may produce data compatible with video output.

1.1.3 Components of the Polarization-difference Camera

The PDI camera is to consist of three major sections. The first is the polarization analyzer that will filter light into orthogonal components based on polarization, each component to be used for enhancing feature detection by reducing the effects of veiled light and highly contrasting background light. The second section is the solid-state imager. It will be used to convert the polarized light signals to electronic signals of proportional magnitude in either a voltage mode or a current mode, map them to various analog circuits for processing, and then digitize the output for use with an external image display system. The third section is the image display system, which will receive the signal output from the solid-state analyzer and transform it to produce image data that can be used to optimally display the images themselves [1].

1.1.4 Research Objectives

I have focused my research on the design of the solid-state imager. The imager, which will be made with complementary metal-oxide semiconductor (CMOS) technology, should have the functionality to amplify input signals and perform arithmetical computations with them. Design considerations should take such things as noise, sensitivity, temperature, and dynamic range of light into account. I have modeled several analog circuits that may be used in the imager and tested them using the Simulation Program with Integrated Circuit Emphasis (SPICE). The output generated from these models should lead to useful insights in the final design of the solid-state imager for the PDI camera.

1.2. Concept of Polarization-Difference Imaging

Polarization-difference imaging presents a way to significantly improve the perception of objects suspended in a scattering medium. All light can be divided into orthogonal pairs based on the direction of a given directional axis of linear polarization. The human visual system is incapable of doing this, and we can only see the combined intensities of all linearly polarized pairs- the polarization-sum, without using visual aids [1]. In this way humans are blind to polarization, which is a common phenomenon in nature.

1.2.1 Polarization of Light

Light tends to be linearly polarized to various degrees when it is reflected from objects of significant size in natural environments. This is in contrast to direct sunlight, which is unpolarized and to produces orthogonal light pairs of equal size when seen through a polarization filter. In a scattering medium, image-forming light represents light reflected from a target object, while veiling light represents light from the background reflected into the path of image-forming light by scatterers of insignificant size (microscopic in most cases) [1]. Image-forming light is generally polarized, at least to some weak degree. Background light and veiling light are generally unpolarized. These are properties that can be usefully exploited by polarization-difference imaging. If one were to devise a way to extract orthogonal pairs of linearly polarized light and subtract the individual components, one could negate the presence of unpolarized light that is present in an equal amount in each component. In a scattering medium, the remaining light would be that which is polarized; a property commonly associated with light reflected from objects [1]. The background light and veiling light that cloud the image of the objects to human eyes could essentially be removed. Feature extraction can be made possible from the direction of polarization and relative intensity that varies over the area of the image. The data from the procedure could be passed on for processing and eventual display. This is the essence of polarization-difference imaging [3].

1.2.2 Effectiveness of Polarization-difference Imaging

Research conducted on polarization-difference imaging has indicated that it is an effective method for target detection and feature extraction for objects suspended in scattering media. It has been experimentally shown that surface features of a target object in a scattering medium that could not be detected using conventional imagery were visible using polarization-difference imagery. Tyo, Rowe, Pugh, and Engheta showed that it was possible to view target objects in such a medium that reflected light with an observable degree of linear polarization of less than 1% [1]. The same study explained that polarization-difference imaging can even be effective when background light is polarized. In this case, one would need to adjust the directional axis of linear polarization used by the filtering mechanism. If the axis is aligned parallel to the direction in which the background light is polarized, the effects of the background light can be removed. Its effectiveness and versatility make polarization-difference imaging a useful way to significantly improve the detection and feature extraction of objects in scattering media [3].

1.3. Solid-State CMOS Imager

Solid-state imagers are commonly used in modern imaging equipment. The imager needed for the polarization-difference camera should be able to transduce the signal intensities of each of the orthogonally polarized light beams that it receives from the filtering mechanism, which will be placed on the chip, into electronic output. Analog circuitry that will be used to add and subtract the signals is also needed.

1.3.1 Benefits of CMOS Technology

The imager has a complementary metal-oxide semiconductor (CMOS) device structure. CMOS allows for many benefits over the charge-coupled device (CCD) technology that is used in many modern imagers.. Since it is the most widely used device structure for very large-scale integrated circuitry, CMOS is widely available and cost effective technology to fabricate. It allows for a great degree of flexibility, as additional circuitry can be implemented on-chip without the compatibility problems encountered with other device structures. CMOS also allows for customizing designs with relative ease [5].

1.3.2 CMOS Active Pixel Sensors

Modern CMOS process improvements, as well as the general benefits of CMOS discussed above, have led us to consider making designs that are classified as active pixel sensors [6]. These sensors make use of active transistors to buffer signal output within the pixels and drive the readout circuitry of the pixel arrays. The arrays themselves can be made very flexible. Currently under consideration is an array of active pixel sensors that can be read out one row at a time. A column of row registers addresses each of the pixels in a row, each of which then sends output to a bottom row of column registers and adjacent analog circuitry. The final output is made up of the two electronic polarization

signals from each pixel, the sum of the two signals (polarization-sum), and the difference of the two signals (polarization-difference). It can be amplified and sent to an analog-to-digital converter to produce digital output. CCDs are currently popular in imagers because they can be highly sensitive and produce high-resolution images, though modern CMOS active pixel sensors are approaching the same level of quality in terms of imaging capabilities [6]. While data from CCD pixel arrays is typically read out one pixel at a time in sequence, the CMOS active pixel array may be designed to allow for random accessibility of pixel data. The ability to address a single pixel or a subsection of pixels in the array could simplify zooming considerably, while power dissipation and speed improvements over typical CCD arrays are possible since entire rows of pixel output may be addressed and processed simultaneously [7]. The ability to make the random-access array, in addition to the several general benefits of the device structure itself (mentioned above), have led us to make CMOS circuit designs for the imager of the polarization-difference camera.

1.3.3 Designs for Components of a CMOS Imager

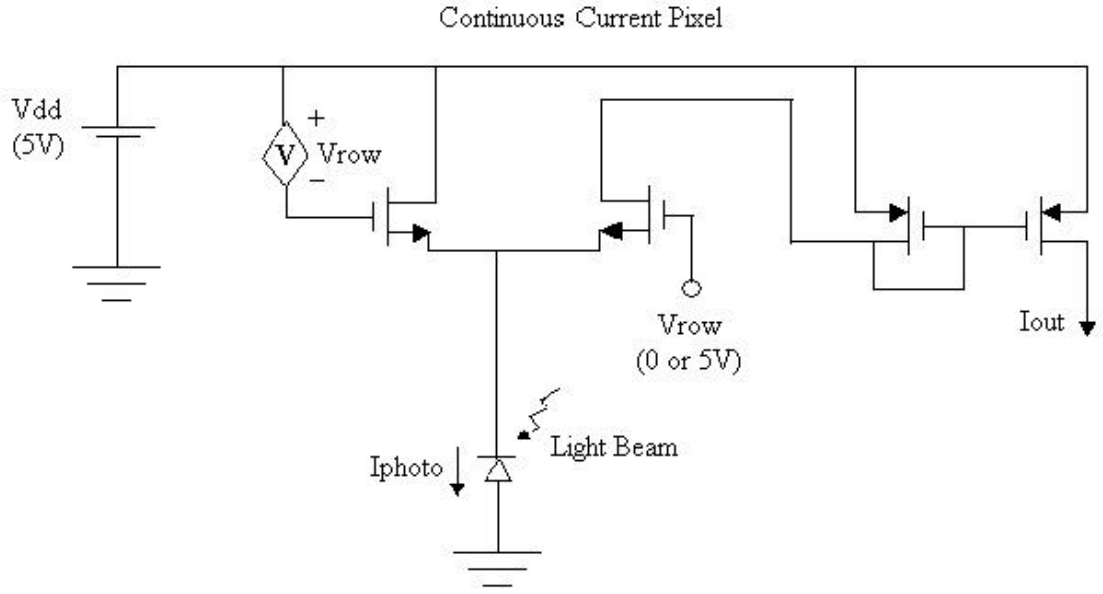
Several designs for the pixel and processing circuitry are being considered for the CMOS imager. We are designing pixels that operate in a current-mode or a voltage-mode. Pixels in the current-mode will produce output signals that are generated from the current that passes through their photodetectors. Pixels in the voltage-mode will produce output signals that are generated from the voltage across their photodetectors. Different image display systems may require either type of output. Some of the designs for parts of the imager are included below. Results of examining the designs are included as well. Design factors such as aspect ratio for transistors and operational biasing are discussed. The temperature range of operation is given. In addition, process factors are given consideration. The designs were modeled using elements made from a 1.2µm n-well CMOS process. Using SPICE, each design was tested using the typical, minimum, and maximum parameter sets. We have concluded the discussion of each of the designs with a brief analysis of the simulation experiments.

2. EXPERIMENTAL RESULTS

2.1. Design of Continuous Current Output Pixel

The continuous current pixel operates in the current mode by mapping the photocurrents generated by the photodiodes (two corresponding to each polarized light beam) to the external processing circuitry. A schematic diagram of half of the pixel is included below. It maps the photocurrent for one of the polarized light beams; the other half of the pixel is identical and produces photocurrent for the complementary polarized beam. The current source marked Iphoto in the diagram represents the photodiode in this half-pixel. It continuously draws a current proportional in magnitude to the light that radiates upon it. In the absence of light, only a negligible leakage current flows through the diode. The photocurrent is the output of the pixel. If the pixel lies within a row (of the larger pixel array) that is being addressed, this output will be read out through the column line to which the pixel is attached. This column line is represented in the

diagram by the line to the extreme right, leading to the downward arrow labeled Iout, which represents the photocurrent output.



The portion of the half-pixel above is divided into two main sections: the section to the upper right of the photodiode maps current to the output when the pixel lies within an addressed row of the pixel array, while the section to the upper left of the photodiode allows current to be drawn when the pixel is not within an addressed row. The voltage source to the extreme left in the diagram, labeled Vdd, supplies power to the entire half-pixel. The input labeled Vrow that is attached to the gate of the NMOS transistor nearest the diode to the right-hand side accepts power supplied to the pixel when it is in a row that is being addressed. A voltage equal to the power supply voltage of the half-pixel (five volts in the diagram) ensures that current is passed through the transistor, which is then sent to the NMOS current-mirror to the right. The mirrored current is the output, which is sent to external processing circuitry. The dependent voltage source V to the left-hand side of the diode takes the same supply voltage, and effectively cuts off the NMOS transistor that it is attached to so that all of the photocurrent passes through the right-hand side to the output. When no power is supplied through Vrow (signifying that the pixel is not lying within an addressed row), the dependent voltage source V takes a value of zero volts, which effectively maps the power supply voltage to the gate NMOS transistor to which it is attached, allowing all of the photocurrent to flow through it while the transistor to the right of the diode is in cut-off mode. The photodiode is operated in reverse-bias mode, and the voltage over it adjusts so that the required photocurrent is passed through it. As this voltage is equal to the source voltage of the NMOS transistors above the diode, care must be taken so that it does not exceed the power supply voltage of the half-pixel.

2.1.1 Modeling and Testing

The half-pixel in the diagram above was modeled and tested using SPICE. Hewlett Packard 1.2µm n-well CMOS transistor models employing typical operating parameters were used. The device parameters for this technology are given in appendix AAA. To test basic operation, the photocurrent Iphoto was allowed to vary from 0uA to 30uA (a realistic range of photocurrents) in steps of 5uA, and the input voltage Vrow was pulsed at 5 volts for 50ms. The temperature of the circuit was kept constant at 25°C. The resulting output current, Iout, was recorded at a time of 20ms into the high pulse voltage of Vrow. Actual data points are provided in the table below. A copy of the SPICE source code for this pixel is given in appendix A.

Iphoto (uA)	Iout (uA)
0.00	$4.81 * 10^{-4}$
5.00	5.00
10.00	10.00
15.00	15.00
20.00	20.00
25.00	25.00
30.00	30.00

Photocurrent and output current in a continuous current pixel

The results of the tests indicate that the pixel operates as expected. It successfully mapped the photocurrent to the output to within less than 1/100 of a microamp. Thus, this design, taken together with the other half corresponding to the complementary polarized light beam, may be considered as a model for a pixel for the PDI camera operating in the current-mode.

2.1.2 Design Evaluation

The continuous current pixel derives its name from the fact that it allows photocurrent to be drawn continuously over the pixel, and that ideally, output can be read out randomly and for any period of time. While this may be very promising, the design above lacks the circuitry required to switch the supply voltage between the two NMOS transistors adjacent to the photodiode with respect to the supplied row voltage. This feature is necessary for current to be mapped to the correct section of the half-pixel, and is dealt with in the above design by implementing the dependent voltage source V. Modeling this mechanism for a real pixel may add to the complexity of the pixel and increase its size, thereby reducing image resolvability. Though pixel size was not a factor that was tested with this model, it must be considered when image quality is taken into account. A test of basic operation indicates that the continuous current pixel may be taken as a possible model for a current-mode pixel to be used in a CMOS imager for a PDI camera.

2.2 Design of Integrated Voltage Pixel

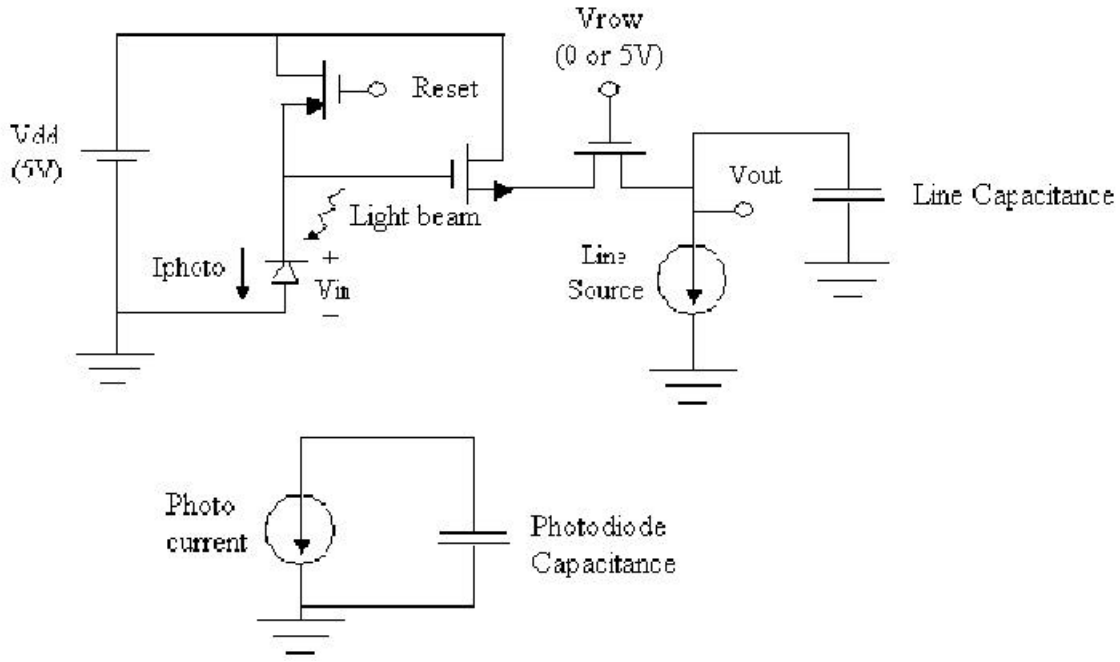
The integrative voltage pixel operates in the voltage-mode by mapping the voltages over the photodiodes in each pixel to external processing circuitry. Photocurrent

is drawn continuously through the photodiode, as it was in the continuous current pixel. Unlike the continuous current pixel, however, the current is not always drawn from the pixel's power source. The photocurrent in this pixel is integrated on the intrinsic capacitance of the photodiode itself, after having been charged to a specified voltage level by the power source. This current, which is proportional to the magnitude of light radiating on the photodiode, is ideally given by the following equation:

$$Iphoto = Cdiode * (dV / dt)$$

Where Cdiode is the total junction capacitance of the photodiode, and (dV / dt) is the change in voltage over the photodiode with respect to time. The voltage is sampled at a constant time interval and mapped to external circuitry. Since the capacitance of the photodiode is constant, and the voltage sampling occurs at a constant interval, the voltage that is mapped to the output of the pixel varies linearly with the photocurrent through the diode. A diagram an integrative voltage half-pixel is given below.

Integrative Voltage Pixel



The smaller diagram below the half-pixel provides a simplified schematic representation of the photodiode. It includes a current source for the photocurrent, and a capacitor that represents the total junction capacitance of the diode. The pixel is powered by the constant voltage source Vdd, located to the extreme left of the pixel diagram. The NMOS transistor that has an input labeled Reset at its gate gives the capacitor an initial charge. This occurs when the Reset voltage is pulsed to a positive value such as the value of the pixel's power supply voltage. While the capacitor is charging, current is also drawn through the transistor to supply the required photocurrent through the photodiode. When the Reset voltage becomes equal to zero, the photocurrent is integrated on the

capacitor, thus depleting the charge on it and lowering the voltage across the photodiode. This voltage appears at the gate of the NMOS transistor to the right of the photodiode in the above diagram. When the switch transistor that has its gate labeled Vrow is given a positive voltage (meaning that the row in which the pixel is situated is being addressed), the voltage across the photodiode is then mapped to the output column line that is attached to the pixel. The current source on the column line and the NMOS transistor that accepts the photodiode voltage at its gate acts as a buffer amplifier. The buffer is necessary due to any parasitic capacitance that may appear on the column output line, which may have the effect of distorting the value of the output voltage. The output voltage is read out from the pixel array through the column line and sent to external processing circuitry.

2.2.1 Modeling and Testing

The half-pixel in the diagram above was modeled and tested using SPICE. Hewlett Packard 1.2µm n-well CMOS transistors models employing typical operating parameters were used. To test basic operation, the photocurrent Iphoto was allowed to vary from 50pA to 300pA in steps of 50pA, and the input voltage Reset was pulsed at 5 volts for a duration of 5ms. The photodiode capacitance was designed to have a value of 1 pF, a realistic value for a total junction capacitance of a photodiode. The temperature of the circuit was kept constant at 25°C. For a discharge time of 13ms, the voltage for over the diode capacitor was sampled for each corresponding photocurrent. This sampled voltage was recorded. Actual data points are provided in the table below. A copy of the SPICE source code for this pixel is given in appendix B.

Iphoto (pA)	Photodiode Voltage (V)
50.00	4.314
100.00	3.665
150.00	3.017
200.00	2.366
250.00	1.718
300.00	1.073

Photocurrent and photodiode voltage in an integrative voltage pixel

To test the operation of the buffer amplifier, the sampled voltages were passed through to the output assuming an ideal row switch. The column output line was given a capacitance of 0.5 pF to simulate actual operation. The output voltages, Vout, are recorded in the table below.

Photodiode Voltage (V)	Output Voltage (V)
4.314	3.434
3.665	2.788
3.017	2.143
2.366	1.495
1.718	0.850
1.073	0.208

Photodiode voltage and output voltage for an integrative voltage pixel

The voltage loss that occurs through the buffer amplifier given the photodiode voltages as input is noteworthy. This loss stays within 30% for the first three entries in the table, but it then becomes significantly greater as the photodiode voltage decreases. While a signal loss of about 10% to 30% is to be expected of this type arrangement, the greater losses may not be sustainable. Additional amplifiers or voltage adders may be necessary to decrease this voltage loss. The overall results of the tests indicate that the pixel operates as expected before the photodiode voltage is buffered and sent to the column output line. A graph of the sampled photodiode voltages over photocurrent was made to verify linear operation. This graph is included in appendix H. It shows that a linear relationship exists. As indicated next to the graph, the linear relationship between the photodiode voltages and the photocurrents is given by the equation:

$$V = (-0.013 * I) + 4.962$$

This equation is very close to that which would be suggested by the following equation, which is a variation of that which was given earlier to describe the ideal operation of the pixel model given a capacitance of 1 pF, a discharge time of 13 ms, and an initial charge of about 5 volts (the power supply voltage of the pixel):

$$Vphoto = (-0.013 * I) + 5.000$$

The small voltage loss that is experienced is due to the fact that the voltage over the photodiode is the same as the source voltage of the NMOS transistor that accepts the Reset input voltage at its gate. Since the drain of the transistor is connected to the 5 volt power supply and the pulsed Reset voltage is equal to 5 volts as well, the source voltage must be somewhat less (approximately equal to the threshold voltage value of the transistor) than this to allow for current flow.

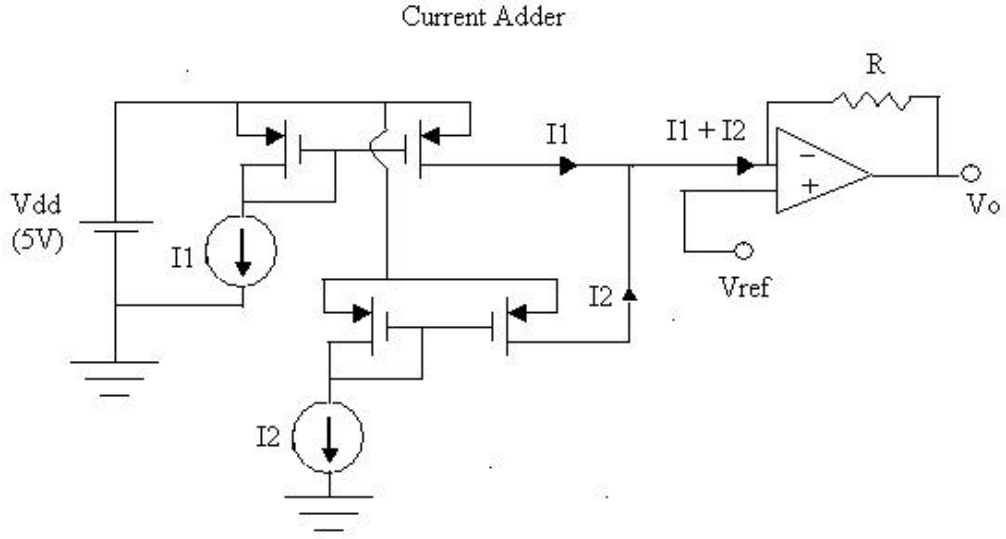
2.2.2 Design Evaluation

The model of the half-pixel was shown to map the voltage over the photodiode for various photocurrents to the column buffer, where signal attenuation problems then occurred. As was mentioned before, additional amplifiers may be used to rectify this problem. Another potential problem relates to the magnitude of photocurrent inputs to the pixel. The photocurrents need to be small enough to ensure that the diode capacitance

does not discharge too quickly. Smaller magnitudes of photocurrent allow for a broader range of signal output since sampling of the diode voltage is done over a constant interval. One way of correcting this problem would be to choose fast sampling rates, or place a current-limiting resistance in the circuit. Of course, these may add to the complexity and size of the pixel. A further complication of this design is the need for a clock mechanism for the pulsing of the Reset voltage and its synchronization with the addressing of the row switches within each pixel. These complexities, however, may be dealt with outside of the pixel and would not necessarily add to the size of the pixels and reduce image quality. Problems with charging the photodiode capacitor to the same voltage for each Reset pulse could reduce image quality, as the sampled photodiode voltages must be compared to a constant initial voltage (the differential must be found with respect to time) to properly correlate with the photocurrent in a linear manner. For this reason, many electronic cameras that make use of charged capacitors in their pixels employ the technique of correlated double sampling, where the initial voltage across the capacitors are sampled along with the voltages that appear after a regular time interval. This mechanism would require extra clock circuitry, but may also be placed outside of the individual pixels. The pixel array structure allows for these clocking mechanisms to be employed for an entire row of pixels, which reduces the need to enlarge the individual pixels to a significant degree. After taking into account the potential problems mentioned, one may begin to consider the integrative voltage pixel as a viable pixel design for a PDI camera operating in the voltage mode.

2.3 Design of Current Adder

The current adder sub-circuit is to be used for producing a polarization-sum image in a PDI camera that has pixels operating in the current-mode. The image, ideally the same as a typical image which maps light intensity spatially, can be used for various purposes. For example, one might compare the image to the polarization-difference image after adjusting for the axes of polarization. A schematic diagram of the circuit is given below.



The two current sources in the diagram represent the two polarized photocurrents generated from a single pixel. The output nodes of the current-mirrors, both sets using PMOS transistors, are connected together so that the sum of both of the reflected photocurrents can be sent to the output of the circuit. The diagram above also includes an operational-amplifier and a resistor for converting the output current into an output voltage if necessary. The following equation shows how the output voltage would be linearly related to the sum of the currents:

$$Vo = Vref + (I1 + I2) * R$$

The circuit was modeled using the SPICE program. Its operation was tested using various fabrication parameters, transistor dimensions, and temperatures. These variables were chosen due to their potential to alter the basic operation of the current-mirrors in the circuit.

2.3.1 Modeling and Testing: Fabrication Parameters

The fabrication parameters used in the circuit modeling included the given typical, maximum, and minimum parameter sets for the Hewlett Packard 1.2µm n-well CMOS fabrication process. The SPICE model parameter codes for these parameter sets are included in appendix C. Since the manufacturer of the circuits and not the designer gives the fabrication parameters, and they are not generally adjustable, one may not be able to use different sets for optimization purposes. It is important, however, to make sure that proper operation can be maintained for the range of fabrication parameter sets.

The following table gives the recorded data points for I1, I2, and Iout (I1 + I2) in the diagram using the typical fabrication parameters. Using the same test currents that were used in the continuous current pixel, I1 and I2 are simultaneously varied from 0.00uA to 30.00uA in steps of 5.00uA. For this test and the others where the fabrication parameters are varied, the aspect ratio for all of the transistors is use is equal to 1.0 with the width of the conducting channel kept fixed at 100.0µm and the temperature is kept constant at 25°C.

I1 (uA)	I2 (uA)	Iout (uA)
0.00	0.00	$9.27 * 10^{-5}$
5.00	5.00	10.00
10.00	10.00	20.00
15.00	15.00	30.00
20.00	20.00	40.00
25.00	25.00	50.00
30.00	30.00	60.00

Input currents I1 and I2 and output currents of a current adder-Typical parameters

As the results indicate, the current adder operates as expected to within less than 1/100 of a microamp of output current.

The next table gives the same recorded data when the set of maximum fabrication parameters are used in the circuit model. No change was made to aspect ratio or temperature.

I1 (uA)	I2 (uA)	Iout (uA)
0.00	0.00	$1.61 * 10^{-5}$
5.00	5.00	9.99
10.00	10.00	19.99
15.00	15.00	29.99
20.00	20.00	39.99
25.00	25.00	49.99
30.00	30.00	59.99

Input currents I1 and I2 and output currents of a current adder-Maximum parameters

As the results indicate, the current adder operates as expected to within 1/100 of a microamp of output current.

The next table gives the same recorded data when the set of minimum fabrication parameters are used in the circuit model. No change was made to aspect ratio or temperature.

I1 (uA)	I2 (uA)	Iout (uA)
0.00	0.00	$6.80 * 10^{-4}$
5.00	5.00	10.00
10.00	10.00	20.00
15.00	15.00	30.00
20.00	20.00	40.00
25.00uA	25.00uA	50.00uA
30.00uA	30.00uA	60.00uA

Input currents I1 and I2 and output currents of a current adder-Minimum parameters

As the results indicate, the current adder operates as expected to within less than 1/100 of a microamp of output current.

The model of the current adder tested successfully when the range of fabrication parameters was varied. Although one does not have control over the actual parameters that would be used if the model were made into a real circuit, the tests above indicate the circuit adder would function as expected using the parameters provided by the circuit manufacturer. The next two tests will examine the operation of the circuit when typical fabrication parameters are used while the aspect ratio of transistors and the temperature of the circuit is varied.

2.3.2 Modeling and Testing: Aspect Ratio

The aspect ratio of the transistors, which is directly proportional to the currents produced by them, was varied to check for possible changes in the circuit operation. Since aspect ratio can be adjusted for at the design level of circuit fabrication, its effect on operation may be considered for circuit optimization. In the following test, the temperature of the circuit was kept constant at 25°C. The input photocurrents of the circuit were arbitrarily chosen to be 10.000μA and 20.000μA. Both represent examples of photocurrents that may be realistically generated. Ideally, the generated sum of the photocurrents is 30.000μA. The aspect ratio was varied by keeping the channel width of the transistor fixed at 100 micrometers while the length was varied from 10.0 to 100.0 micrometers in increments of 10.0 micrometers. The table below includes the results of this test.

Channel Length (μm)	Iout (μA)
10.0	30.043
20.0	30.005
30.0	30.002
40.0	30.001
50.0	30.000
60.0	30.000
70.0	30.000
80.0	30.000
90.0	30.000
100.0	30.000

Conducting channel length and output current for a current adder

The results suggest that the operation of the current adder is accurate within less than 1/1000 of a microamp of output current when the aspect ratio is kept within 1.0 and 2.0 (and the width of the conducting channels in the transistors equals 100um). The generated current sum becomes progressively larger and less accurate than the ideal sum as the aspect ratio is allowed to increase. This suggests that a low optimal aspect ratio from a point of view of matching layer values of W and L is preferred. Mismatching was not considered with this simulation due to the lack of data.

2.3.3 Modeling and Testing: Temperature

The temperature of the circuit may lead to further changes in overall operation due to its effect on the currents produced in the transistors. Examination of the effects of temperature can lead to important conclusions on the versatility of the circuit in various operating environments. One may then be able to determine its overall functionality in the PDI camera. For testing purposes, the two input photocurrents were again chosen to be 10.00μA and 20.00μA, and the aspect ratio of the transistors was kept at 1.0 with the

width of the conducting channel fixed at 100.0µm. The temperature in the circuit model was varied from 0.0°C to 200.0°C in increments of 20.0°C. The table below includes the results of this test.

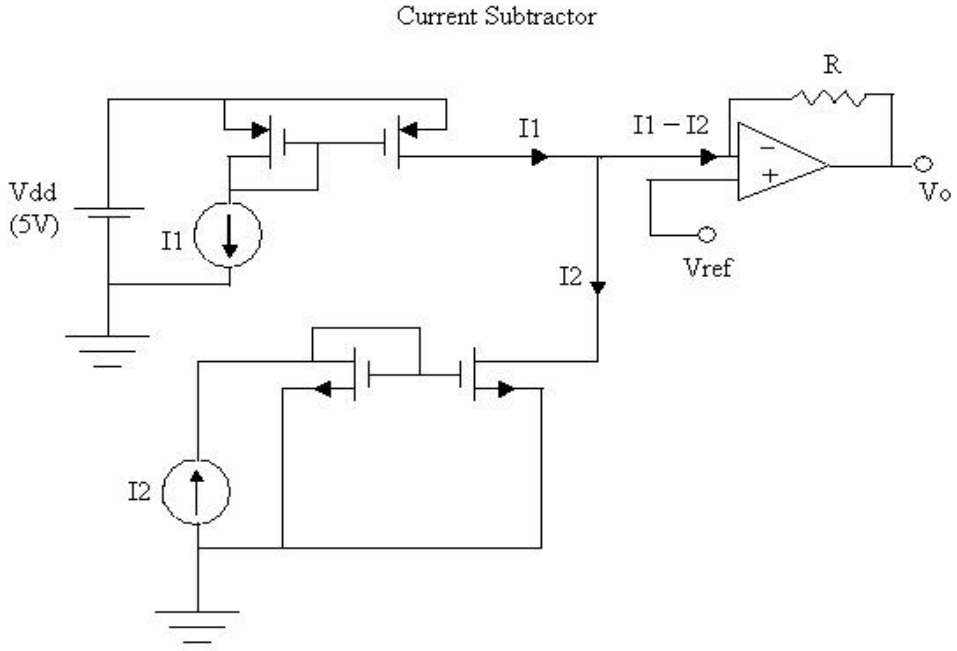
Circuit Temperature (°C)	Iout (uA)
0.0	30.000
20.0	30.000
40.0	30.000
60.0	30.000
80.0	30.000
100.0	30.001
120.0	30.003
140.0	30.017
160.0	30.081
180.0	30.340
200.0	31.294

Circuit temperature and output current for a current adder

The results of the test suggest that the circuit operates accurately within 1/1000 of a microamp of output current when the circuit temperature is kept between 0°C and 100°C. The generated current sum becomes progressively larger and less accurate than the ideal sum as the temperature is allowed to increase past 100°C. This suggests that the current adder should be used in environments with moderate temperatures, and that caution should be taken when the circuit is to operate in high temperatures.

2.4 Design of Current Subtractor

The current subtractor sub-circuit is to be used for producing a polarization-difference image in a PDI camera that has pixels operating in the current-mode. As was discussed previously, it is this polarization-difference image that may allow for improved imaging of objects suspended in scattering media. The camera produces this image by subtracting the two complementary polarized photocurrents generated in each pixel. A schematic diagram of the circuit is given below.



One may note that the design of the current subtractor is quite similar to that of the current adder with the exception that one of the current-mirror sets is made from NMOS transistors. Again, the two output nodes of the current-mirrors are connected, but this time, the difference is sent to the output of the circuit. The operational amplifier and resistor are included in the diagram for the purpose of converting the current output into a proportional voltage if necessary. The following equation shows how the output voltage would be linearly related to the difference of the currents:

$$Vo = Vref + (I1 - I2) * R$$

The current subtractor was modeled using SPICE. To maintain consistency, the same variables that were tested using the current adder model were also tested using the current subtractor model. Fabrication parameters, aspect ratio, and temperature were each varied to examine their effect on the operation of the circuit.

2.4.1 Modeling and Testing: Fabrication Parameters

The Hewlett Packard 1.2µm n-well CMOS process was used again in determining the fabrication parameters for the transistors used in the circuit parameters. The operation of the circuit was tested using the typical, maximum, and minimum parameter sets. The SPICE model parameter codes for each of the sets are included in appendix D. A discussion on the motivation for testing the circuit operation using the given range of fabrication parameters is included above in the section on the current adder.

The following table gives the recorded data points for I1, I2, and Iout (I1 - I2) in the diagram using the typical fabrication parameters. The test currents that were used, I1 and I2, are simultaneously varied. I1 is varied from 0.00μA to 30.00μA in steps of 5.00μA while I2 is varied from 0.00μA to 45.00μA in steps of 7.50μA. For this test and the others where the fabrication parameters are varied, the aspect ratio for all of the transistors is use is equal to 1.0 with the width of the conducting channel kept fixed at 100.0μm and the temperature is kept constant at 25°C.

I1 (μA)	I2 (μA)	Iout (μA)
0.00	0.00	$3.33 * 10^{-5}$
5.00	7.50	-2.50
10.00	15.00	-5.00
15.00	22.50	-7.50
20.00	30.00	-10.00
25.00	37.50	-12.50
30.00	45.00	-15.00

Input currents I1 and I2 and output currents of a current subtractor- Typical parameters

As the results indicate, the current subtractor operates as expected to within less than 1/100 of a microamp of output current.

The next table gives the same recorded data when the set of maximum fabrication parameters are used in the circuit model. No change was made to aspect ratio or temperature.

I1 (uA)	I2 (uA)	Iout (uA)
0.00	0.00	$-3.93 * 10^{-6}$
5.00	7.50	-2.50
10.00	15.00	-5.00
15.00	22.50	-7.50
20.00	30.00	-10.00
25.00	37.50	-12.50
30.00	45.00	-15.00

Input currents I1 and I2 and output currents of a current subtractor-Maximum parameters

As the results indicate, the current subtractor operates as expected to within less than 1/100 of a microamp of output current.

The next table gives the same recorded data when the set of minimum fabrication parameters are used in the circuit model. No change was made to aspect ratio or temperature.

I1 (uA)	I2 (uA)	Iout (uA)

0.00	0.00	$-3.04 * 10^{-3}$
5.00	7.50	-2.50
10.00	15.00	-5.00
15.00	22.50	-7.50
20.00	30.00	-9.99
25.00	37.50	-12.49
30.00	45.00	-14.99

Input currents I1 and I2 and output currents of a current adder-Minimum parameters

2.4.2 Modeling and Testing: Aspect Ratio

The aspect ratio of the transistors was varied to check for possible changes in the circuit operation in the same manner as the current adder was tested. Further discussion is included in the current adder section. For testing purposes, the input photocurrents of the circuit were arbitrarily chosen to be 10.00μA and 20.00μA. Both represent examples of photocurrents that may be realistically generated. Ideally, the generated sum of the photocurrents is -10.00μA. The aspect ratio was varied by keeping the channel width of the transistor fixed at 100.0 micrometers while the length was varied from 10.0 to 100.0 micrometers in increments of 10.0 micrometers. The set of typical fabrication parameters was used and temperature was kept constant at 25°C in the circuit model. The table below includes the results of this test.

Channel Length (μA)	Iout (μA)
10.0	-9.982
20.0	-9.998
30.0	-9.999
40.0	-10.000
50.0	-10.000
60.0	-10.000
70.0	-10.000
80.0	-10.000
90.0	-10.000
100.0	-10.000

Conducting channel length and output current for a current subtractor

The results suggest that the operation of the current adder is accurate within less than 1/1000 of a microamp of output current when the aspect ratio is kept within 1.0 and 2.5 (and the width of the conducting channels in the transistors equals 100um). The generated current difference becomes progressively smaller and less accurate than the ideal difference as the aspect ratio is allowed to increase. This suggests a low optimal aspect ratio for the transistors in the circuit, probably not much larger than 1.0.

2.4.3 Modeling and Testing: Temperature

As was mentioned in the section on the current adder, temperature changes in the circuit may lead to changes in overall operation due to its effect on the currents produced in the transistors. Further discussion on the importance of testing the effects of temperature changes on circuit operation is given in that section. For testing purposes, the two input photocurrents were again chosen to be 10.00μA and 20.00μA, and the aspect ratio of the transistors was kept at 1.0 with the width of the conducting channel fixed at 100.0μm. The temperature in the circuit model was varied from 0.0°C to 200.0°C in increments of 20.0°C. The expected result is for Iout to equal –10.000μA. The table below includes the results of this test.

Circuit Temperature (°C)	Iout (uA)
0.0	-10.000
20.0	-10.000
40.0	-10.000
60.0	-10.000
80.0	-10.000
100.0	-10.000
120.0	-9.998
140.0	-9.988
160.0	-9.941
180.0	-9.751
200.0	-9.053

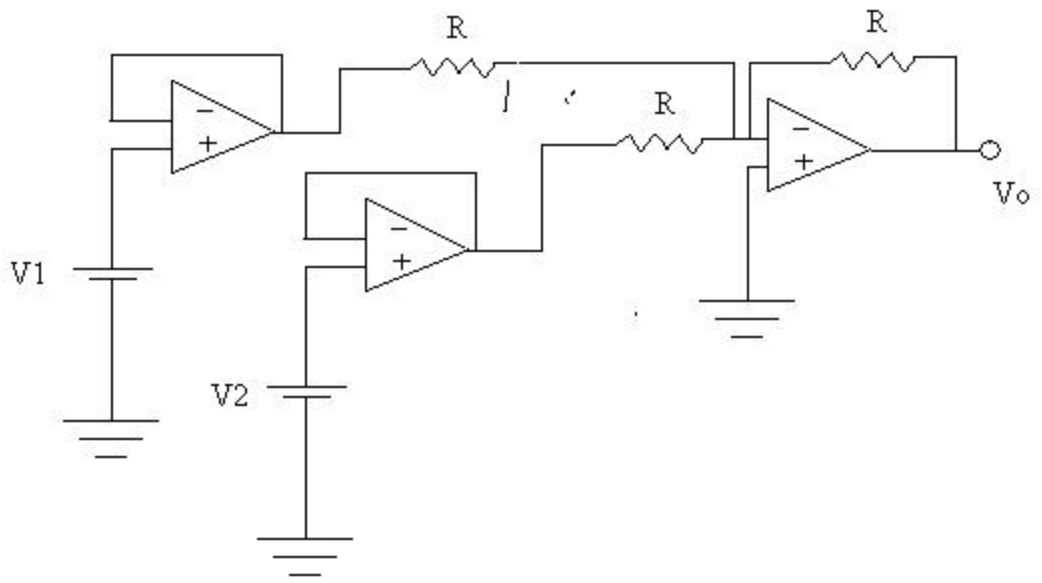
Circuit temperature and output current for a current adder

The results of the test suggest that the circuit operates accurately within 1/1000 of a microamp of output current when the circuit temperature is kept between 0°C and 100°C. The generated current difference becomes progressively smaller and less accurate than the ideal difference as the temperature is allowed to increase past 100°C. This suggests that the current subtractor should be used in environments with moderate temperatures, and that caution should be taken when the circuit is to operate in high temperatures.

2.5. Design of Voltage Adder

The voltage adder sub-circuit is to be used for producing a polarization-sum image in a PDI camera that has pixels operating in the voltage-mode. As was stated in the section about the current adder, a polarization-sum image is ideally the same as a typical image that maps light intensity spatially and can be used for various important purposes. A schematic diagram of the circuit is given below.

Voltage Adder



The two voltage sources in the diagram represent the voltage output of the two polarized photocurrents generated from a single pixel. They are connected to two operational amplifiers that operate as buffers. These buffers are needed to prevent drawing current from the pixels and changing their operation. Each output of the buffers is connected to identical resistors, and are then sent to the inverting and non-inverting inputs of another operational amplifier that operates with feedback. All resistors in the model are identical. The output voltage Vo of the adder is linearly related to the sum of the input voltages V1 and V2 and is ideally given by the following equation:

$$Vo = - (V1 + V2)$$

The output voltage is the inverted sum of the input voltages, and may be sent through and inverter (not shown) to retrieve the voltage sum.

The above diagram was modeled and tested using SPICE. Identical CMOS operational amplifiers were employed and each was fabricated using the Hewlett Packard 1.5mm n-well CMOS process. One property of the operational amplifiers used in this circuit is that their output saturates at voltages close to 50μV. This is somewhat undesirable since the voltage input from the pixels may generally be in the range of about 0 to 5.00 volts. Amplifiers that can scale these input voltages by a decreasing factor of about 1μV may thus be necessary for proper operation of the designed voltage adder. The SPICE program made it possible to test the circuit using various fabrication parameters for the transistors included in the operational amplifiers. It was also used in testing circuit operation for a range of temperatures. These variables were chosen due to their potential to alter the basic operation of the current-mirrors in the circuit.

2.5.1 Modeling and Testing: Fabrication Parameters

The fabrication parameters used in the testing the circuit included the given typical, maximum, and minimum parameter sets for the Hewlett Packard 1.2µm n-well CMOS fabrication process. The SPICE model parameter codes for these sets are included in appendix E. As was previously mentioned, the manufacturer of the circuits and not the designer gives the fabrication parameters, and one may not be able to use different sets for optimization purposes. It is important, however, to make sure that proper operation can be maintained for the range of fabrication parameter sets.

The following table gives the recorded data points for V1, V2, and Vo (V1 + V2) in the diagram using the typical fabrication parameters. Using scaled voltage output that could be acquired from the integrative voltage pixel, V1 and V2 are simultaneously varied from 0.00µV to 5.00µA in steps of 0.500µA. For this test and the others where the fabrication parameters are varied, the aspect ratio for all of the transistors included in the operational amplifiers are kept constant at their original values and the temperature is kept constant at 25°C.

V1 (µV)	V2 (µV)	Vo (µV)
0.000	0.000	0.000
0.500	0.500	1.061
1.000	1.000	2.022
1.500	1.500	2.983
2.000	2.000	3.943
2.500	2.500	4.904
3.000	3.000	5.865
3.500	3.500	6.826
4.000	4.000	7.787
4.500	4.500	8.748
5.000	5.000	9.708

Scaled input voltages V1 and V2 and output voltages of a voltage adder- Typical parameters

The results indicate that the voltage adder operates as expected to within 3/10 of a microvolt of output voltage. The output becomes less accurate as the applied voltages increase. An additional set of amplifiers may be needed to correct this problem.

The next table gives the same recorded data when the set of maximum fabrication parameters are used in the circuit model. No change was made to aspect ratio or temperature.

V1 (μA)	V2 (μA)	Vo (μA)
0.00	0.00	0.000
0.500	5.00	1.078
1.000	10.00	2.036
1.500	15.00	2.995
2.000	20.00	3.952
2.500	25.00	4.914
3.000	30.00	5.874
3.500	3.500	6.835
4.000	4.000	7.796
4.500	4.500	8.757
5.000	5.000	8.753

Scaled input voltages V1 and V2 and output voltage of a voltage adder-Maximum parameters

As the results indicate, the current adder operates as expected to within 3/10 of a microvolt of output voltage.

The next table gives the same recorded data when the set of minimum fabrication parameters are used in the circuit model. No change was made to aspect ratio or temperature.

V1 (μA)	V2 (μA)	Vo (μA)
0.00	0.00	0.000
0.500	5.00	1.059
1.000	10.00	2.019
1.500	15.00	2.978
2.000	20.00	3.937
2.500	25.00	4.899
3.000	30.00	5.858
3.500	3.500	6.820
4.000	4.000	7.781
4.500	4.500	8.745
5.000	5.000	9.706

Scaled input voltages V1 and V2 and output voltage of a voltage adder- Minimum parameters

As the results indicate, the current adder operates as expected to within 3/10 of a microvolt of output voltage.

2.5.2 Modeling and Testing: Temperature

Basic operation was tested next by varying the temperature of the circuit. The temperature of operation of the transistors in the circuits may lead to further changes in overall operation due to its effect on the currents produced. As was stated before,

examining the effect of temperature on a circuit can lead to important conclusions on the versatility of the circuit in various operating environments. And as was the case with both the current adder and current subtractor, the temperature of this circuit model was varied from 0ºC to 200ºC in increments of 20ºC. For testing purposes, the two input voltages were chosen to be 4.00μV and 2.00μV, and the aspect ratios of the transistors included in the operational amplifiers were kept constant at their original values. Typical transistor fabrication parameters were employed. The table below includes the results of this test. Ideally, V_o should be equal to 6.000μV.

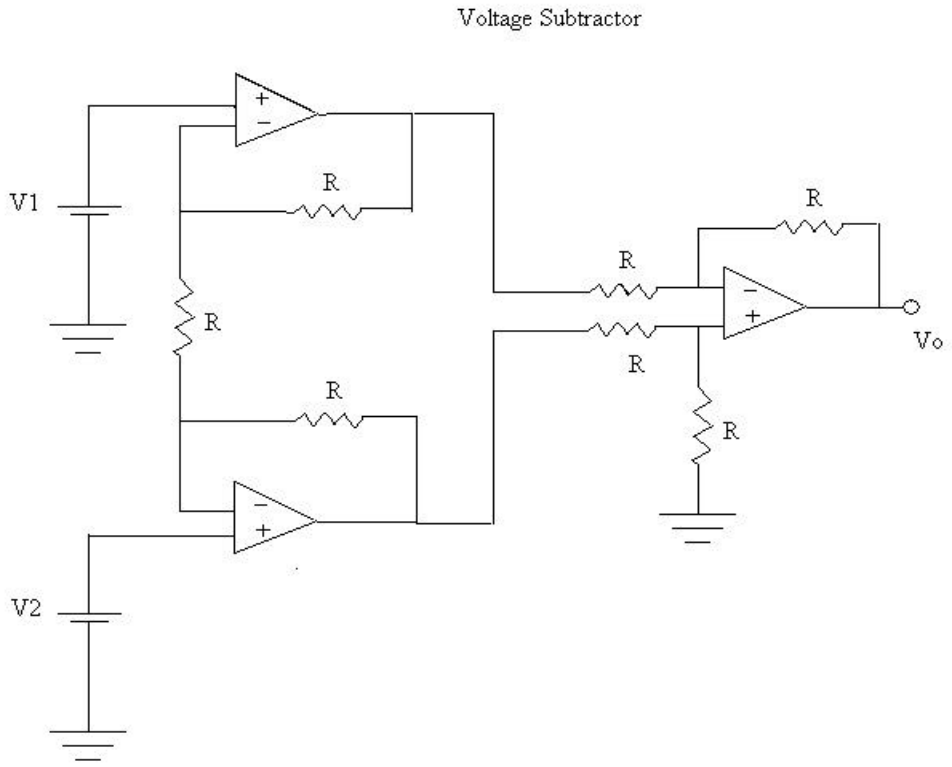
Circuit Temperature (ºC)	Vo (μV)
0.0	5.886
20.0	5.870
40.0	5.853
60.0	5.836
80.0	5.820
100.0	5.804
120.0	5.794
140.0	5.895
160.0	8.474
180.0	56.101
200.0	702.296

Circuit temperature and output voltage for a voltage adder

The results indicate that the circuit model is best suited for moderate temperatures. At room temperature, the output voltage is within 2/10 of its ideal value. Considerable distortion occurs at very high temperatures (above 180°C). This suggests that the voltage adder should be used in environments with moderate temperatures, and that caution should be taken when the circuit is to operate in high temperature environments.

2.6 Design of Voltage Subtractor

The voltage subtractor sub-circuit is to be used for producing a polarization-difference image in a PDI camera that has pixels operating in the voltage-mode. As was stated in the section about the current subtractor, the polarization-difference image will allow for improved imaging of objects suspended in scattering media by rejecting common-mode background light. A schematic diagram of the circuit is given below.



The two voltage sources in the diagram represent the voltage output of the two polarized photocurrents generated from a single pixel. They are connected to the non-inverting inputs of two operational amplifiers that operate with feedback loops connected to their inverting inputs. The output of these operational amplifiers is mapped into the familiar instrumentation amplifier configuration, which allows for the accurate subtraction of the input signals. All resistors in the sub-circuit model are identical. The ideal output voltage Vo of the adder is a linearly related to the sum of the input voltages V1 and V2 and is given by the following equation:

$$Vo = - (V1 - V2) * (2)$$

The output voltage is the inverted difference between the two input voltages, and the output is increased by a factor of two. This output may be sent through an inverter and an amplifier (both not shown) to retrieve the desired ideal voltage difference. .

The above diagram was modeled and tested using SPICE. Identical CMOS operational amplifiers were employed and each was fabricated using the Hewlett Packard 1.2µm n-well CMOS process. One property of the operational amplifiers used in this circuit is that their output saturates at voltages close to 50µm. This is somewhat undesirable since the voltage input from the pixels will generally be in the range of about 0 to 5.00 volts. Amplifiers that can scale these input voltages by a factor of about 1µm may thus be necessary for proper operation of the designed voltage adder. The SPICE program made it possible to test the circuit using various fabrication parameters for the

transistors included in the operational amplifiers. It was also used in testing circuit operation for a range of temperatures. These variables were chosen due to their potential to alter the basic operation of the current-mirrors in the circuit.

2.6.1 Modeling and Testing: Fabrication Parameters

The fabrication parameters used in the testing the circuit included the given typical, maximum, and minimum parameter sets for the Hewlett Packard 1.2µm n-well CMOS fabrication process. The SPICE model parameter codes for these parameter sets are included in appendix F. As was previously mentioned, the manufacturer of the circuits and not the designer gives the fabrication parameters, and one may not be able to use different sets for optimization purposes. It is important, however, to make sure that proper operation can be maintained for the range of fabrication parameter sets.

The following table gives the recorded data points for V1, V2, and Vo (V1 + V2) in the diagram using the typical fabrication parameters. Using scaled voltage output that could be acquired from the integrative voltage pixel, V1 and V2 are simultaneously varied from 0.00µV to 5.00µA in steps of 0.500µA. For this test and the others where the fabrication parameters are varied, the aspect ratio for all of the transistors included in the operational amplifiers are kept constant at their original values and the temperature is kept constant at 25°C. The output shown below has been corrected for the effects of the inversion and voltage gain produced from the ideal model discussed above.

V1 (µA)	V2 (µA)	Vo (µA)
0.000	0.000	0.000
1.500	1.000	0.594
3.000	2.000	1.093
4.500	3.000	1.590
6.000	4.000	2.086
7.500	5.000	2.583
9.000	6.000	3.079
10.500	7.000	3.576
12.000	8.000	4.073
13.500	9.000	4.569
15.000	10.000	5.066

Scaled input voltages V1 and V2 and output voltages of a voltage subtractor- Typical parameters

The results indicate that the voltage subtractor operates as expected to within less than 1/10 of a microvolt of output voltage. The basic design of the voltage subtractor (with typical parameters) works reasonably well.

The next table gives the same recorded data when the set of maximum fabrication parameters are used in the circuit model. No change was made to aspect ratio or temperature.

V1 (μA)	V2 (μA)	Vo (μA)
0.000	0.000	0.000
1.500	1.000	0.622
3.000	2.000	1.101
4.500	3.000	1.599
6.000	4.000	2.095
7.500	5.000	2.590
9.000	6.000	3.083
10.500	7.000	3.579
12.000	8.000	4.080
13.500	9.000	4.578
15.000	10.000	5.072

Scaled input voltages V1 and V2 and output voltage of a voltage subtractor-Maximum parameters

As the results indicate, the current adder operates as expected to within 1/10 of a microvolt of output voltage.

The next table gives the same recorded data when the set of minimum fabrication parameters are used in the circuit model. No change was made to aspect ratio or temperature.

V1 (μA)	V2 (μA)	Vo (μA)
0.000	0.000	$2.41 * 10^{-5}$
1.500	1.000	0.590
3.000	2.000	1.089
4.500	3.000	1.585
6.000	4.000	2.080
7.500	5.000	2.576
9.000	6.000	3.077
10.500	7.000	3.571
12.000	8.000	4.063
13.500	9.000	4.562
15.000	10.000	5.061

Scaled input voltages V1 and V2 and output voltage of a voltage subtractor – Minimum parameters

As the results indicate, the current adder operates as expected to within 1/10 of a microvolt of output voltage.

2.6.2 Modeling and Testing: Temperature

Basic operation was tested next by varying the temperature of the circuit. The temperature of operation of the transistors in the circuits may lead to further changes in

overall operation due to its effect on the currents produced. As was stated before, examining the effect of temperature on a circuit can lead to important conclusions on the versatility of the circuit in various operating environments. And as was the case with both the current adder and current subtractor, the temperature of this circuit model was varied from 0ºC to 200ºC in increments of 20ºC. For testing purposes, the two input photocurrents were again chosen to be 4.00μV and 2.00uV, and the aspect ratios of the transistors included in the operational amplifiers were kept constant at their original values. Typical transistor fabrication parameters were employed. The table below includes the results of this test. The ideal value for V_o should be 2.000μV

Circuit Temperature (ºC)	Vo (μV)
0.0	2.096
20.0	2.089
40.0	2.082
60.0	2.076
80.0	2.070
100.0	2.067
120.0	2.092
140.0	2.340
160.0	5.518
180.0	53.410
200.0	641.896

Circuit temperature and output voltage for a voltage subtractor

The results indicate that the design for the voltage subtractor works reasonably well when tested in moderate temperatures. At about room temperature (20°C) it works to within less than 1/10 of its ideal value. Considerable distortion occurs at high temperatures (above 160°C). This suggests that the voltage adder should be used in environments with moderate temperatures, and that caution should be taken when the circuit is to operate in high temperature environments.

3. CONCLUSIONS/DISCUSSION

Polarization-difference imaging has been shown to be an effective technique for improving target-detection in media characterized by scattered light. A practical camera that can integrate polarization-difference imaging techniques to produce useful imagery could enhance the performance of several applications that depend upon reliable imagery in such media. Designs for several key components of a CMOS imager to be used with a polarization-difference camera have been presented and analyzed using the Simulation Program with Integrated Circuit Emphasis (SPICE).

Designs for components of the CMOS imager were made for circuitry that may operate in a voltage-mode or a current-mode. Thus, designs of pixels, signal adders, and signal subtractors have been included in pairs; one design for a voltage-mode imager and one design for a current-mode imager. The continuous current pixels maps photocurrent

to external circuitry base upon the voltage of the row address pins of the pixel array. The integrated voltage pixel integrates photocurrent onto the intrinsic capacitance within the photodiodes of the pixel and relies upon sampling to output a voltage that is linearly related to the current passing through the photodiodes. The photodiode capacitance must be charged to a pre-specified level in regular intervals to allow for sustained operation. The current adder utilizes a simple design involving PMOS current mirrors that sum the electronically transduced polarization signals together and map the result to the output. The current subtractor involves a similar design, but takes the difference of the signal currents by using a PMOS current mirror that pushes one of the signal currents toward the output and a NMOS current mirror that sinks the other signal current from it (thereby forming the difference of the signals). Both the current adder and the current subtractor designs tested successfully under varied fabrication parameters and varied circuit temperatures. The voltage adder employed CMOS operational amplifiers to buffer input photodiode voltage signals and to add the signals in a standard summing configuration. The voltage subtractor also uses CMOS operational amplifiers to buffer input signals and to subtract them in a typical instrumentation amplifier differencing configuration. Both the voltage adder and the voltage subtractor designs tested successfully under the varied fabrication parameters and varied circuit temperatures. The SPICE input codes used in the analysis of each of the designs have been included in the appendix section.

While the goal of creating simple designs for key components of a CMOS imager to be used in a polarization-difference imaging camera has been accomplished, several important factors about such an imager have yet to be determined. Practical measures such of size and cost of the designs remain to be determined. The intricacies of the pixel array structure implementing these designs must be investigated. A full examination of the parasitic effects that arise in circuit operation has not been conducted. Measures that may improve upon the current designs also need to be investigated. The CMOS operational amplifiers that were used in the voltage adder and voltage subtractor designs, for example, may be optimized for more precise operation. These are just a few of the critical factors one must consider in determining the feasibility of the presented designs. It is hoped that continued testing and design improvements will lead to a design of a fully functional and versatile CMOS imager.

4. ACKNOWLEDGEMENTS

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APPENDIX A

SPICE Source Code – Continuous Current Pixel (typical fabrication parameters)

Continuous Current Pixel

```
* Source Elements

vdd 1 0 dc 5v
vrow 7 0 pulse (0v 5v 10ms 1ms 1ms 50ms 60ms)  * vrow input is given a voltage pulse
*to test pixel switching from on to off.  Voltage pulse *models stimulation from
photoarray row switches.

enrow 1 2 7 0 1
vcl 9 3 dc 0v      * voltage sources with zero voltage across used for checking currents
vcr 5 3 dc 0v
vco 8 0 dc 0v
ibias 3 4 dc 0a    * ”ibias” is the simulated photocurrent
vcb 4 0 dc 0v

* Line Capacitance

cline 8 0 .5pf      * simulated capacitance of output line in photoarray

* Transistors

m1 6 7 5 5 nmos l=2u w=10u
m2 6 6 1 1 pmos l=100u w=100u
m3 8 6 1 1 pmos l=100u w=100u
m4 1 2 9 9 nmos l=2u w=10u

* Transistor Models

**NMOS

.model nmos nmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
+tpg=1 vto=0.7860 delta=6.9670e-01 ld=1.6470e-07 kp=9.6379e-05
+uo=591.7 theta=8.1220e-02 rsh=8.5450e+01 gamma=0.5863
+nsub=2.7470e+16 nfs=1.98e+12 vmax=1.7330e+05 eta=4.3680e-02
+kappa=1.3960e-01 cgdo=4.0241e-10 cgso=4.0241e-10
+cgbo=3.6144e-10 cj=3.8541e-04 mj=1.1854 cjsw=1.3940e-10
+mjsw=0.125195 pb=0.800000
```

```
**PMOS

.model pmos pmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
+tpg=-1 vto=-0.9056 delta=1.5200e+00 ld=2.2000e-08 kp=2.9352e-05
+uo=180.2 theta=1.2480e-01 rsh=1.0470e+02 gamma=0.4863
+nsub=1.8900e+16 nfs=3.46e+12 vmax=3.7320e+05 eta=1.6410e-01
+kappa=9.6940e+00 cgdo=5.3752e-11 cgso=5.3752e-11
+cgbo=3.3650e-10 cj=4.8447e-04 mj=0.5027 cjsw=1.6457e-10
+mjsw=0.217168 pb=0.850000

* Analysis Request

.tran 0.2ms 70ms sweep ibias 0ua 30ua 5ua   *simulated photocurrent swept from 0µA to
*20µA in steps of 5 µA

* Output Request

.print tran v(4) i(vco) i(vcr) i(vcl)

.end
```

APPENDIX B

SPICE Source Code – Integrative Voltage Pixel (typical fabrication parameters)

Integrative Voltage Pixel

```
* Source Elements

vdd 1 0 dc 5v
vrow 2 0 pulse (5v 0v 5ms 1ms 1ms 25ms 30ms)  * Pulsed row access voltage
iph 4 0 dc 0pa        * Simulated photocurrent
ibias 5 0 10ua         * Bias current generated from pixel array; necessary to buffer output
*voltage

vcheck 3 4 dc 0v    * Voltage sources that act as short circuits; implemented for
*verification purposes

vc2 7 0 dc 0v

* Capacitors

cdiode 4 7 1pf         * simulated capacitance of photodiode
cline 5 0 0.5pf         * simulated capacitance of output line

* Transistors

m1 1 2 3 3 nmos l=1.2u w=4u          * NMOS transistor data
m2 1 4 5 5 nmos l=2u w=10u

* Transistor Models

** NMOS

.model nmos nmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
model nmos nmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
+tpg=1 vto=0.7860 delta=6.9670e-01 ld=1.6470e-07 kp=9.6379e-05
+uo=591.7 theta=8.1220e-02 rsh=8.5450e+01 gamma=0.5863
+nsub=2.7470e+16 nfs=1.98e+12 vmax=1.7330e+05 eta=4.3680e-02
+kappa=1.3960e-01 cgdo=4.0241e-10 cgso=4.0241e-10
+cgbo=3.6144e-10 cj=3.8541e-04 mj=1.1854 cjsw=1.3940e-10
+mjsw=0.125195 pb=0.800000

** PMOS
```

```
.model pmos pmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
+tpg=-1 vto=-0.9056 delta=1.5200e+00 ld=2.2000e-08 kp=2.9352e-05
+uo=180.2 theta=1.2480e-01 rsh=1.0470e+02 gamma=0.4863
+nsub=1.8900e+16 nfs=3.46e+12 vmax=3.7320e+05 eta=1.6410e-01
+kappa=9.6940e+00 cgdo=5.3752e-11 cgso=5.3752e-11
+cgbo=3.3650e-10 cj=4.8447e-04 mj=0.5027 cjsw=1.6457e-10
+mjsw=0.217168 pb=0.850000

* Analysis Request

.tran 0.2ms 45ms sweep iph 50pa 300pa 50pa  * photocurrent swept while row access
*voltage is pulsed

* Output Request

.print tran v(2) v(3) v(5) *i(vcheck) i(vc2)

. end
```

APPENDIX C

SPICE Source Code – Current Adder (typical fabrication parameters)

Current Adder

```
* Source Elements

vdd 1 0 dc 5v          * Power supply voltage
vref 6 0 dc 1v
vi1 8 7 dc 0v          * First polarized input signal
vi2 3 7 dc 0v          * Second polarized input signal
vtot 7 9 dc 0v
vref1 10 0 dc 0v       ***  All other voltage supplies used in checking operation ***
vref2 14 0 dc 0v
vcom 12 0 dc 0v

* Input Current Sources

gaa 4 10 12 0 1
gbb 13 14 12 0 2

* Current Mirrors (MOSFETS used in modeling)

m1 4 4 1 1 pmos l=la w=wa * l=10u w=100u  *(name, drain gate source substrate)
m2 8 4 1 1 pmos l=la w=wa * l=10u w=100u
m3 13 13 1 1 pmos l=la w=wa * l=10u w=100u
m4 3 13 1 1 pmos l=la w=wa  *  l=10u w=100u

* Transistor Models

** NMOS

.model nmos nmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
+tpg=1 vto=0.7860 delta=6.9670e-01 ld=1.6470e-07 kp=9.6379e-05
+uo=591.7 theta=8.1220e-02 rsh=8.5450e+01 gamma=0.5863
+nsub=2.7470e+16 nfs=1.98e+12 vmax=1.7330e+05 eta=4.3680e-02
+kappa=1.3960e-01 cgdo=4.0241e-10 cgso=4.0241e-10
+cgbo=3.6144e-10 cj=3.8541e-04 mj=1.1854 cjsw=1.3940e-10
+mjsw=0.125195 pb=0.800000

** PMOS
```

```
.model pmos pmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
+tpg=-1 vto=-0.9056 delta=1.5200e+00 ld=2.2000e-08 kp=2.9352e-05
+uo=180.2 theta=1.2480e-01 rsh=1.0470e+02 gamma=0.4863
+nsub=1.8900e+16 nfs=3.46e+12 vmax=3.7320e+05 eta=1.6410e-01
+kappa=9.6940e+00 cgdo=5.3752e-11 cgso=5.3752e-11
+cgbo=3.3650e-10 cj=4.8447e-04 mj=0.5027 cjsw=1.6457e-10
+mjsw=0.217168 pb=0.850000

* Ideal Opamp

eopamp 5 0 6 7 1e6          * Produces output voltage (optional)

* Resistors

rgen 9 5 10                 * Necessary for voltage conversion of output (optional)
rcom 12 0 1000              * Not included in model; allows for checking

* Analysis Request

.dc vcom 0uv 10uv 5uv sweep data=d1      * Sweeps input voltages in model

* Output Request

.print dc i(vi1) i(vi2) i(vtot)          * Data presentation

.end
```

APPENDIX D

SPICE Source Code – Current Subtractor (typical fabrication parameters)

Current Subtractor

```
* Source Elements

Vdd 1 0 DC 5V                 * Power supply voltage
Vref 6 0 DC 1V
Vi1 8 7 DC 0V
Vi2 7 3 DC 0V          ***  All other voltage supplies used in checking operation ***
Vtot 7 9 DC 0V
Vref1 10 0 DC 0V
Vref2 1 11 DC 0V
Vcom 12 0 DC 0V

* Input Current Sources

Gaa 4 10 12 0 1               * First polarized input signal
Gbb 11 2 12 0 2               * Second polarized input signal

* Current Mirrors  (MOSFETS used in modeling)

M1 4 4 1 1 pmos L=la W=wa
M2 8 4 1 1 pmos L=la W=wa
M3 2 2 0 0 nmos L=la W=wa
M4 3 2 0 0 nmos L=la W=wa

* Transistor Models

** NMOS

.MODEL NMOS NMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08 XJ=0.200000U
+TPG=1 VTO=0.7860 DELTA=6.9670E-01 LD=1.6470E-07 KP=9.6379E-05
+UO=591.7 THETA=8.1220E-02 RSH=8.5450E+01 GAMMA=0.5863
+NSUB=2.7470E+16 NFS=1.98E+12 VMAX=1.7330E+05 ETA=4.3680E-02
+KAPPA=1.3960E-01 CGDO=4.0241E-10 CGSO=4.0241E-10
+CGBO=3.6144E-10 CJ=3.8541E-04 MJ=1.1854 CJSW=1.3940E-10
+MJSW=0.125195 PB=0.800000


** PMOS
```

```
.MODEL PMOS PMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08 XJ=0.200000U
+TPG=-1 VTO=-0.9056 DELTA=1.5200E+00 LD=2.2000E-08 KP=2.9352E-05
+UO=180.2 THETA=1.2480E-01 RSH=1.0470E+02 GAMMA=0.4863
+NSUB=1.8900E+16 NFS=3.46E+12 VMAX=3.7320E+05 ETA=1.6410E-01
+KAPPA=9.6940E+00 CGDO=5.3752E-11 CGSO=5.3752E-11
+CGBO=3.3650E-10 CJ=4.8447E-04 MJ=0.5027 CJSW=1.6457E-10
+MJSW=0.217168 PB=0.850000

* Ideal OpAmp

Eopamp 5 0 6 7 1e6          * Produces output voltage (optional)

* Resistors

Rgen 9 5 10                 * Necessary for voltage conversion of output (optional)
Rcom 12 0 1000              * Not included in model; allows for checking

* Analysis Request

.DC Vcom 0uV 10uV 5uV       * Sweeps input voltages in model

* Output Request

.Print DC I(Vi1) I(Vi2) I(Vtot)        * Data presentation

.end
```

APPENDIX E

SPICE Source Code – Voltage Adder (typical fabrication parameters)

Voltage Adder

```
* Source Elements

vcom 99 0 0v
ev1 12 0 99 0 1
ev2 22 0 99 0 1

*eopamp 4 0 0 3 1e6

* Central Opamp

* Power Supplies

vdd 4 0 dc 5v
vss 5 0 dc -5v

* Front-end Stage

m1 7 1 6 4 pmos l=8u w=120u
m2 8 0 6 4 pmos l=8u w=120u
m3 7 7 5 5 nmos l=10u w=50u
m4 8 7 5 5 nmos l=10u w=50u
m5 6 9 4 4 pmos l=10u w=150u

* Second Gain Stage

m6 3 8 5 5 nmos l=10u w=100u
m7 3 9 4 4 pmos l=10u w=150u

* Current Source Biasing Stage

m8 9 9 4 4 pmos l=10u w=150u
iref 9 5 25ua

* Compensation Network

cc 8 10 10pf
r 10 3 10k
```

*** Buffer1

* Front-end Stage

m11 17 13 16 4 pmos l=8u w=120u
m12 18 12 16 4 pmos l=8u w=120u
m13 17 17 5 5 nmos l=10u w=50u
m14 18 17 5 5 nmos l=10u w=50u
m15 16 19 4 4 pmos l=10u w=150u

* Second Gain Stage

m16 13 18 5 5 nmos l=10u w=100u
m17 13 19 4 4 pmos l=10u w=150u

* Current Source Biasing Stage

m18 19 19 4 4 pmos l=10u w=150u
iref1 19 5 25ua

* Compensation Network

cc1 18 110 10pf
ra 110 13 10k

*** Buffer2

* Front-end stage

m21 27 23 26 4 pmos l=8u w=120u
m22 28 22 26 4 pmos l=8u w=120u
m23 27 27 5 5 nmos l=10u w=50u
m24 28 27 5 5 nmos l=10u w=50u
m25 26 29 4 4 pmos l=10u w=150u

* Second Gain Stage

m26 23 28 5 5 nmos l=10u w=100u
m27 23 29 4 4 pmos l=10u w=150u

* Current Source Biasing Stage

m28 29 29 4 4 pmos l=10u w=150u
iref2 29 5 25ua

* Compensation Network

cc2 28 210 10pf
rb 210 23 10k

* Transistor Models

** NMOS

.model nmos nmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
+tpg=1 vto=0.7860 delta=6.9670e-01 ld=1.6470e-07 kp=9.6379e-05
+uo=591.7 theta=8.1220e-02 rsh=8.5450e+01 gamma=0.5863
+nsub=2.7470e+16 nfs=1.98e+12 vmax=1.7330e+05 eta=4.3680e-02
+kappa=1.3960e-01 cgdo=4.0241e-10 cgso=4.0241e-10
+cgbo=3.6144e-10 cj=3.8541e-04 mj=1.1854 cjsw=1.3940e-10
+mjsw=0.125195 pb=0.800000

** PMOS

.model pmos pmos level=3 phi=0.600000 tox=2.1200e-08 xj=0.200000u
+tpg=-1 vto=-0.9056 delta=1.5200e+00 ld=2.2000e-08 kp=2.9352e-05
+uo=180.2 theta=1.2480e-01 rsh=1.0470e+02 gamma=0.4863
+nsub=1.8900e+16 nfs=3.46e+12 vmax=3.7320e+05 eta=1.6410e-01
+kappa=9.6940e+00 cgdo=5.3752e-11 cgso=5.3752e-11
+cgbo=3.3650e-10 cj=4.8447e-04 mj=0.5027 cjsw=1.6457e-10
+mjsw=0.217168 pb=0.850000

* Resistors

r1 13 1 100
r2 23 1 100
r3 1 3 100
rcom 99 0 100
rgen 50 0 100

* Analysis Request

.dc vcom 0v 5uv 0.5uv

* Output Request

.print dc v(12) v(22) v(50)
.end

APPENDIX F

SPICE Source Code – Voltage Subtractor (typical fabrication parameters)

Voltage Subtractor

```
* Source Elements

Vcom 99 0 DC 0V
E1 2 0 99 0 3
E2 12 0 99 0 2
E3 900 0 23 0 .5

*** OpAmps ***

*OpAmp1

*Power supplies
Vdd 4 0 DC 5V
Vss 5 0 DC -5V

*front-end stage
M1 7 1 6 4 pmos L=8u W=120u
M2 8 2 6 4 pmos L=8u W=120u
M3 7 7 5 5 nmos L=10u W=50u
M4 8 7 5 5 nmos L=10u W=50u
M5 6 9 4 4 pmos L=10u W=150u

*Second gain stage
M6 3 8 5 5 nmos L=10u W=100u
M7 3 9 4 4 pmos L=10u W=150u

*Current source biasing stage
M8 9 9 4 4 pmos L=10u W=150u
Iref 9 5 25uA

*Compensation network
Cc 8 10 10pF
R 10 3 10k

*Model statements

.MODEL NMOS NMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08 XJ=0.200000U
```

+TPG=1 VTO=0.7860 DELTA=6.9670E-01 LD=1.6470E-07 KP=9.6379E-05
+UO=591.7 THETA=8.1220E-02 RSH=8.5450E+01 GAMMA=0.5863
+NSUB=2.7470E+16 NFS=1.98E+12 VMAX=1.7330E+05 ETA=4.3680E-02
+KAPPA=1.3960E-01 CGDO=4.0241E-10 CGSO=4.0241E-10
+CGBO=3.6144E-10 CJ=3.8541E-04 MJ=1.1854 CJSW=1.3940E-10
+MJSW=0.125195 PB=0.800000

.MODEL PMOS PMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08 XJ=0.200000U
+TPG=-1 VTO=-0.9056 DELTA=1.5200E+00 LD=2.2000E-08 KP=2.9352E-05
+UO=180.2 THETA=1.2480E-01 RSH=1.0470E+02 GAMMA=0.4863
+NSUB=1.8900E+16 NFS=3.46E+12 VMAX=3.7320E+05 ETA=1.6410E-01
+KAPPA=9.6940E+00 CGDO=5.3752E-11 CGSO=5.3752E-11
+CGBO=3.3650E-10 CJ=4.8447E-04 MJ=0.5027 CJSW=1.6457E-10
+MJSW=0.217168 PB=0.850000

*OpAmp2

*front-end stage
M11 17 11 16 4 pmos L=8u W=120u
M12 18 12 16 4 pmos L=8u W=120u
M13 17 17 5 5 nmos L=10u W=50u
M14 18 17 5 5 nmos L=10u W=50u
M15 16 19 4 4 pmos L=10u W=150u

*Second gain stage
M16 13 18 5 5 nmos L=10u W=100u
M17 13 19 4 4 pmos L=10u W=150u

*Current source biasing stage
M18 19 19 4 4 pmos L=10u W=150u
Iref1 19 5 25uA

*Compensation network
Cc1 18 110 10pF
Ra 110 13 10k

*OpAmp3

*front-end stage
M21 27 21 26 4 pmos L=8u W=120u
M22 28 22 26 4 pmos L=8u W=120u
M23 27 27 5 5 nmos L=10u W=50u
M24 28 27 5 5 nmos L=10u W=50u
M25 26 29 4 4 pmos L=10u W=150u

*Second gain stage

```
M26 23 28 5 5 nmos L=10u W=100u
M27 23 29 4 4 pmos L=10u W=150u

*Current source biasing stage
M28 29 29 4 4 pmos L=10u W=150u
Iref2 29 5 25uA

*Compensation network
Cc2 28 210 10pF
Rb 210 23 10k

*Resistors

Rcom 99 0 1
R1 1 11 1kohm
R2 1 3 500
R3 11 13 500
R4 3 21 1kohm
R5 13 22 1kohm
R6 21 23 1kohm
R7 22 0 1kohm
Rt 900 0 1

*Analysis

.DC Vcom 0V 10uV 0.5uV

*Output Request

.Print DC V(2) V(12) V(900) V(23)

.option post
.end
```

APPENDIX G

SPICE Source Code – Transistor Model Parameter Sets

Hewlett Packard 1.2µm n-well CMOS transistors

TYPICAL PARAMETERS

* NMOS

```
.MODEL NMOS NMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08 XJ=0.200000U
+TPG=1 VTO=0.7860 DELTA=6.9670E-01 LD=1.6470E-07 KP=9.6379E-05
+UO=591.7 THETA=8.1220E-02 RSH=8.5450E+01 GAMMA=0.5863
+NSUB=2.7470E+16 NFS=1.98E+12 VMAX=1.7330E+05 ETA=4.3680E-02
+KAPPA=1.3960E-01 CGDO=4.0241E-10 CGSO=4.0241E-10
+CGBO=3.6144E-10 CJ=3.8541E-04 MJ=1.1854 CJSW=1.3940E-10
+MJSW=0.125195 PB=0.800000
```

* PMOS

```
.MODEL PMOS PMOS LEVEL=3 PHI=0.600000 TOX=2.1200E-08 XJ=0.200000U
+TPG=-1 VTO=-0.9056 DELTA=1.5200E+00 LD=2.2000E-08 KP=2.9352E-05
+UO=180.2 THETA=1.2480E-01 RSH=1.0470E+02 GAMMA=0.4863
+NSUB=1.8900E+16 NFS=3.46E+12 VMAX=3.7320E+05 ETA=1.6410E-01
+KAPPA=9.6940E+00 CGDO=5.3752E-11 CGSO=5.3752E-11
+CGBO=3.3650E-10 CJ=4.8447E-04 MJ=0.5027 CJSW=1.6457E-10
+MJSW=0.217168 PB=0.850000
```

MAXIMUM PARAMETERS

* NMOS

```
.MODEL NMOS NMOS LEVEL=3
PHI=0.600000 TOX=2.1500E-08 XJ=0.200000U +TPG=1 VTO=0.8063
DELTA=9.4090E-01 LD=1.3540E-07 KP=1.0877E-04 +UO=680.4
THETA=8.3620E-02 RSH=109.3 GAMMA=0.5487 +NSUB=2.3180E+16
NFS=1.98E+12
VMAX=1.8700E+05 ETA=5.5740E-02 +KAPPA=5.9210E-02 CGDO=3.2469E-10
CGSO=3.2469E-10 +CGBO=3.7124E-10 CJ=3.1786E-04 MJ=1.0148
CJSW=1.3284E-10 +MJSW=0.119521 PB=0.800000
```

* PMOS

```
.MODEL PMOS PMOS LEVEL=3 PHI=0.600000
```

TOX=2.1500E-08 XJ=0.200000U +TPG=-1VTO=-0.9403 DELTA=8.5790E-01
LD=1.1650E-09 KP=3.4276E-05 +UO=214.4 THETA=1.4010E-01 RSH=122.2
GAMMA=0.5615 +NSUB=2.4270E+16 NFS=3.46E+12 VMAX=3.9310E+05
ETA=1.5670E-01 +KAPPA=9.9990E+00 CGDO=2.7937E-12 CGSO=2.7937E-12
+CGBO=3.5981E-10 CJ=4.5952E-04 MJ=0.4845 CJSW=2.7917E-10
+MJSW=0.365250 PB=0.850000

MINIMUM PARAMETERS

* NMOS

.MODEL NMOS NMOS LEVEL=3
PHI=0.600000 TOX=2.0500E-08 XJ=0.200000U +TPG=1 VTO=0.8147
DELTA=3.0170E-05 LD=1.7540E-07 KP=8.9765E-05 +UO=532.9
THETA=9.0470E-02 RSH=1.5870E+01 GAMMA=0.6654 +NSUB=3.7840E+16
NFS=5.5000E+12 VMAX=1.7140E+05 ETA=6.4550E-02 +KAPPA=5.6190E-02
CGDO=4.4318E-10 CGSO=4.4318E-10 +CGBO=3.2044E-10 CJ=3.1786E-04
MJ=1.0148 CJSW=1.3284E-10 +MJSW=0.119521 PB=0.800000

* PMOS

.MODEL PMOS PMOS LEVEL=3 PHI=0.600000
TOX=2.0500E-08 XJ=0.200000U +TPG=-1 VTO=-0.9189 DELTA=2.3190E+00
LD=1.0440E-08 KP=3.3521E-05 + UO=199.0 THETA=1.7940E-01 RSH=25.0000
GAMMA=0.4124 +NSUB=1.4540E+16 NFS=5.0000E+12 VMAX=5.4640E+05
ETA=2.1090E-01 + KAPPA=9.3670E+00 CGDO=2.6379E-11 CGSO=2.6379E-11 +
CGBO=2.8996E-10 CJ=4.6135E-04 MJ=0.4831 CJSW=1.8681E-10 +
MJSW=0.315030 PB=0.850000

APPENDIX H

Voltage – Current Relationship of the Integrated Voltage Pixel