CMOS ACTIVE PIXEL SENSOR FOR A POLARIZATION-DIFFERENCE CAMERA

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Gregory J. Barlow (Electrical Engineering) – North Carolina State University
Advisors: Dr. Nader Engheta and Dr. Jan Van der Spiegel

ABSTRACT

Polarization-sensitive vision is well documented as serving in navigation for many animals, but some types of biological polarization-sensitive vision may enhance object visibility in scattering media. Because neither the human eye nor conventional cameras are polarization-sensitive, artificial polarization vision systems must be designed to exploit the polarization of light; artificial polarization-difference imaging has been shown to be capable of enhancing target detection in scattering media. Previous polarization-sensitive cameras required external processing, were not real-time, and used relatively large amounts of power. A CMOS active pixel sensor is presented for use in a low power, portable, real-time polarization-difference camera. Pixels were designed for integration with a diffractive optical element polarization analyzer. Column readout circuits include fixed pattern noise suppression. In addition, a scaling methodology to enhance system performance and to correct for non-ideal polarization analyzers is presented.

1. INTRODUCTION

Humans rely heavily on their visual systems to understand the world around them. Human vision is based on brightness and color, which are extremely efficient under normal conditions. [1] In optically scattering media, however, such as underwater, in fog, or in rain, variations of brightness and color are low, diminishing object contrast and lowering the effectiveness of the visual system. [2] While polarization-sensitive vision is well documented as serving in many invertebrate navigation systems, Rowe et al. hypothesize that the green sunfish uses polarization vision to enhance target detection underwater. [3] Artificial polarization-sensitive vision has been shown to enhance the visibility of target objects in scattering media, using a method called polarization-difference imaging (PDI), inspired by the visual system of the green sunfish. [4]

Polarization-sensitive cameras have been previously demonstrated, but have not been designed to operate at full video rates. [4,5,6,7] In addition, these schemata require the use of significant external computing resources, limiting the portability of the system. Nor have these cameras been designed for low power use. The design of a low power, portable, real-time polarization-sensitive electronic camera-on-a-chip is desirable for use in a variety of applications.

This paper covers a variety of areas related to the design and implementation of a polarization-difference camera. Section 2 gives a brief review of polarization and PDI,

background on electronic cameras and diffractive optical elements (DOE), and information on charged coupled devices and CMOS pixels. Section 3 covers the overall design of the camera. Section 4 addresses the design and layout of the CMOS active pixel sensor (APS) used in this camera, with specific consideration of the design constraints of a PDI camera. Section 5 contains the designs of the readout circuitry for the camera and methods of fixed pattern noise (FPN) reduction. Section 6 details the operation of the camera, with some specifications for control, timing, and drive systems. Section 7 addresses intensity scaling to correct for the non-ideal DOE polarization analyzer. Section 8 gives the simulation results for the designed circuits, while Section 9 contains discussion of results and project conclusions. Future work and recommendations are addressed in Section 10.

2. BACKGROUND

2.1 Polarization

Light has three properties detectable by vision systems: intensity, wavelength, and polarization. While the human eye can perceive both intensity and wavelength, it is polarization-blind. For this reason, conventional electronic cameras are not designed to extract polarization information from a scene. [5]

Light is a transverse electromagnetic wave; its electric and magnetic fields are orthogonal to the direction of propagation. The path traced by the tip of the electric field as the wave propagates defines the polarization of light. Light sources, such as the sun, are usually randomly polarized, while the media that the light encounters tend to alter its polarization.

2.2 Biological Basis

Polarization vision has been extensively studied in many classes of invertebrates. Bees, ants, and other invertebrates use polarization for navigation. [2] While some vertebrates are capable of extracting polarization information from visible light, the physical mechanism is not as well understood as in invertebrate systems. The sensitivity of the green sunfish to variations in polarization led to the hypothesis that polarization was used to enhance underwater vision. [3] The potential for vision enhancement makes polarization sensitivity desirable to incorporate into electronic cameras.

2.3 Polarization-difference Imaging

PDI is one method of extracting polarization information from a scene. In this method, images of a scene are captured at two orthogonal linear polarizations. The pixel-by-pixel sum of the two images forms the polarization-sum (PS), and the pixel-by-pixel difference of the two images forms the polarization-difference (PD). [2] Color is used to map the PD into the visual realm. [8]

If the two image intensity distributions are symbolized as $I_1(i,j)$ and $I_2(i,j)$, where (i,j) represents the pixel location and I_1 and I_2 have orthogonal linear polarizations, then the PS and PD are as follows:

$$_{PS}I(i,j) = I_1(i,j) + I_2(i,j) \quad (1a)$$
$$_{PD}I(i,j) = I_1(i,j) - I_2(i,j) \quad (1b)$$

The PS image is equivalent to a conventional image if the linear polarizer is ideal. For non-ideal linear polarizers, corrective scaling must be implemented. It should be noted that the PD image depends on the polarization axes. [2]

PDI is qualitatively better than conventional imaging for target detection in scattering media; detection enhancement has been demonstrated at observable degrees of polarization of less than 1%. [4] PDI is inherently capable of common-mode rejection for background light, which further enhances target detection. Because PDI only requires relatively simple computations, it is extremely suitable for use in a polarization sensitive electronic camera.

2.4 Polarization Camera

Previous polarization-sensitive cameras were not real-time, though near-video rates have been achieved. [4,5,6,7] Previous polarization-sensitive cameras have also required intensive external processing. PDI is a suitable method for use in a real-time electronic camera-on-a-chip which is polarization-sensitive.

A polarization-difference camera extends the functionality of a normal digital electronic camera. A conventional electronic camera generally consists of eight stages. [9] These are (1) optical collection of photons via a lens, (2) discrimination of photons, generally based on wavelength (3) detection of photons via a photodiode or photogate, (4) readout of detectors, (5) timing, control, and drive electronics, (6) signal processing electronics, including FPN, (7) analog to digital conversion, and (8) interface electronics. The order of these stages is not necessarily fixed; some signal processing may occur after analog to digital conversion.

2.5 Diffractive Optical Elements

A DOE is a pattern of microstructures that can transform light in a predetermined manner. [10] For example, a Fresnel zone lens DOE can be used to focus light. While the Fresnel zone lens requires a variation of the height of the surface, a sub-wavelength binary DOE can exhibit the same behavior. [11] Figure 1 shows images of both types of lenses. In addition, sub-wavelength binary DOEs are polarization selective, which is advantageous for this project. The DOE designed for this project focuses the incoming light along a line parallel to the grooves of the DOE. This DOE is polarization sensitive.

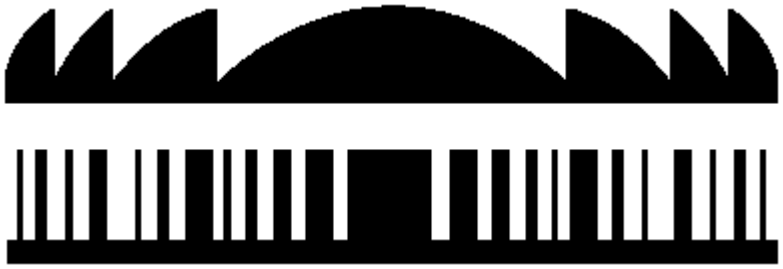

Figure 1 - (a) Fresnel zone lens and (b) sub-wavelength binary lens

2.6 Image Sensors

The imager technology used in an electronic camera is instrumental in determining the capabilities of the final system. Low noise, large array sizes, high frame rates, and power dissipation are preferred for a polarization-difference camera.

2.6.1 Charge-coupled Device Image Sensors

Charge-coupled device (CCD) technology, currently the most popular sensor technology, is capable of producing high-quality images. [9] Small, low-resolution CCD cameras are also relatively inexpensive. CCD technology's relative freedom from FPN is one of its most attractive characteristics. However, CCD-based systems often consume several watts of power, can be accessed only a single pixel at a time, and are difficult to integrate with processing circuitry.

2.6.2 CMOS Image Sensors

MOS image sensors were demonstrated in the 1960's, but work fell off with the introduction of the CCD, which displayed much less FPN than MOS sensors. [9] The need for smaller and less expensive imaging technology has led to a resurgence in the popularity of CMOS image sensors. CMOS imager technology also has the advantage of low power, random and row based pixel access, and easy integration with processing circuitry. There are three main approaches to CMOS pixels: passive pixels, photodiode APSs, and photogate APSs. APSs can be designed for operation in either voltage or current-mode.

2.6.3 CMOS Passive Pixel Sensors

The passive pixel sensor is very simple, consisting of a photodiode and a transfer transistor. [9] Passive pixel sensors have high quantum efficiency and extremely small pixel size; however, noise levels are quite high, and this pixel type does not scale well.

2.6.4 CMOS Active Pixel Sensors

An active pixel includes at least one active transistor within the pixel cell. [12] An active amplifier within the pixel helps to improve performance over that of the passive pixel, allowing larger arrays and faster readout speeds. Since the amplifier within a pixel draws power only when the pixel is being read out, power dissipation remains low. Many APSs have been designed, some with very high quality and extremely high frame rates. [13-23] Active pixels are either photodiode or photogate based; readout is either voltage-mode or current-mode.

2.6.5 Photodiode APS

The most common photodiode-type active pixel, shown in Figure 2, includes three transistors and the photodiode. A reset transistor resets the photodiode, and a source follower buffers the voltage on the photodiode. A row select transistor enables readout to the column bus. This design has high quantum efficiency, as the diode is not covered by polysilicon. [12] Because the integration and reset nodes are the same, correlated double sampling (CDS), a FPN suppression method, is more difficult to implement.

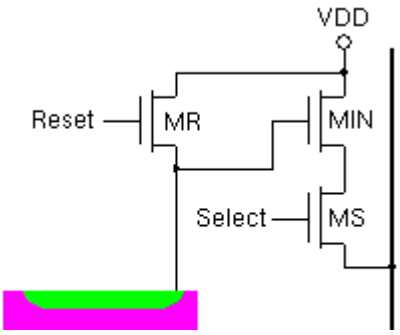

Figure 2 – Schematic of CMOS photodiode APS

2.6.6 Photogate APS

Identical to the photodiode-type active pixel in the layout of the reset transistor, source follower, and row select transistor, the photogate-type active pixel uses a photogate followed by a transfer gate in place of the photodiode. [9] The quantum efficiency of a photogate is less than that of a photodiode, because of the polysilicon covering. [12] FPN is also higher. The primary advantage of the photogate-type active pixel is its ability to do CDS, which is very effective in suppressing reset noise, 1/f noise, and FPN. [13]

2.6.7 Voltage and Current-mode APS

A majority of the active pixels that have been investigated are voltage-mode pixels. [13-18] These pixels have demonstrated excellent performance, with high speeds and low noise levels. [15,16] FPN suppression techniques have been developed, and on-chip analog-to-digital conversion has been demonstrated. [18]

While less work has been done on current-mode active pixels, many have been demonstrated. [19-23] Current-mode active pixels show potential for improvements in readout speed and lower readout noise, though none yet seriously rival voltage-mode pixels. Effective FPN reduction for current-mode active pixels is still being investigated. On-chip analog-to-digital conversion has been presented. [19,22]

3. CAMERA DESIGN

A polarization-difference camera extends the necessary functions of a normal digital electronic camera. After the optical collection of photons with a lens, DOE polarization analyzers are used to separate the light into polarized components. A pixel then converts the photons to electrons. For each pixel of output, it is necessary for the sensor array to have two input pixels, one for each component of polarization. After detection, the pixels are read out on a column bus into CDS circuitry, which suppresses FPN. The analog signal is then converted to a digital signal using an on-chip analog-to-digital converter. Because it is not possible to design an ideal DOE polarization analyzer, output signal corrective scaling is necessary. Scaling to enhance system performance is also desirable. For each signal pair, the output signal undergoes a combined scaling process that incorporates both corrective and performance-enhancing scaling. The scaled intensities are then summed and differenced to obtain the polarization-sum and polarization-difference. The polarization-sum is effectively the intensity for that pixel. The polarization-difference is mapped into color. Video interface electronics then display the image. A schematic of the stages of the polarization-difference camera is shown in Figure 3.

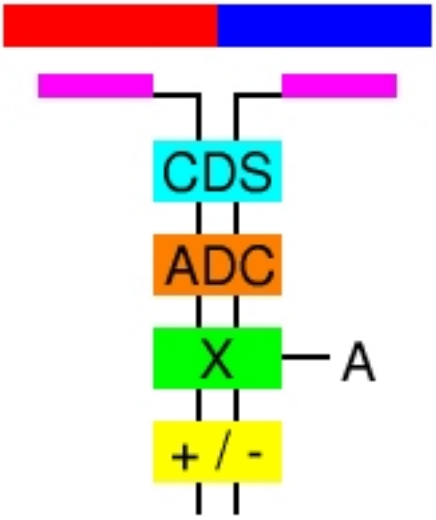

Figure 3 - Stages of the polarization-difference camera

This work focused on the design of the APS, the readout circuitry, and the scaling methodology to correct for the non-ideal nature of the polarization analyzer.

4. CMOS APS

The pixel type selected for this design was a voltage-mode photogate APS. Using a voltage-mode pixel simplified FPN suppression circuitry and layout considerations. The use of photogate-type active pixels enabled the use of CDS.

4.1 Design

Figure 4 shows a schematic of the pixel circuit design. This is one of the most common types of APSs. [12] The photogate is separated from the floating diffusion node by a transfer gate, which allows for CDS. The transfer gate is biased at a constant voltage, while the photogate is pulsed. (See Section 6) The pixel unit also contains a reset

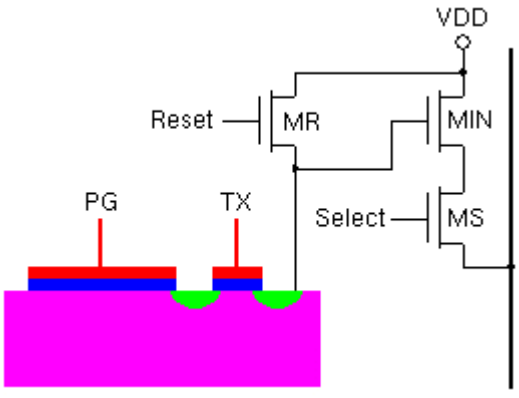

Figure 4 - Schematic of CMOS photogate APS

transistor, an in-pixel source follower, and a row selection transistor.

While a standard electronic camera has one input pixel for every pixel of output resolution, this polarization camera requires two inputs for every output, since each "half pixel" represents one component of the linear polarization. The sum and difference of the two pixels form the polarization sum and polarization difference, which make up the polarization-difference image. The diffractive optical element layer above the sensor array is arranged in stripes; neighboring pixels in a given row are overlaid with DOEs oriented orthogonal to one another, as shown in Figure 5.

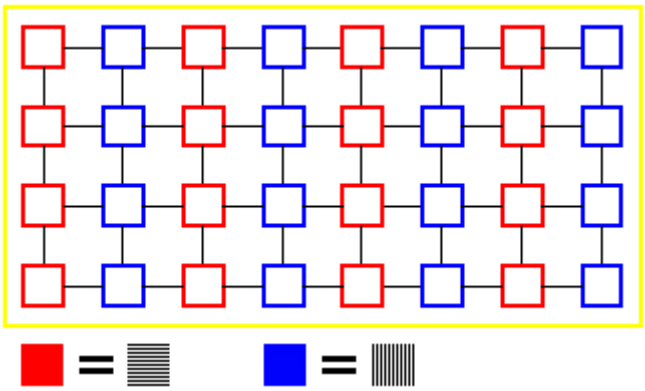

Figure 5 - Schematic for orientation of the DOE overlay of the pixel array

4.2 Layout

The orientation of the DOEs in a striped pattern places certain constraints on the layout of the APS. The DOE focuses incoming light along a line in the center of the DOE, and the pixel should be designed to capture as much light as possible. To maximize the photogate area and to keep the pixel vertically symmetrical for integration with the DOE, the photogate is T-shaped, as seen in Figure 6. A light shield, which also acts as the power rail, covers all areas of the pixel except the photogate. This limits crosstalk between neighboring pixels. The pixel has been designed to overlap with its neighboring pixel to maximize detector area. The integration of the pixels with the DOE is shown in Figure 7. The left DOEs focus light on the vertical section of the corresponding pixels, while the right DOE's focus light on the horizontal section of the corresponding pixels. When combined into the sensor array, each pixel is 18 microns by 18 microns using an AMI 0.6μm double poly, three metal process. The total photogate area in each pixel is ~130 square microns. All transistors in the pixel have W/L ratios of 6/2.

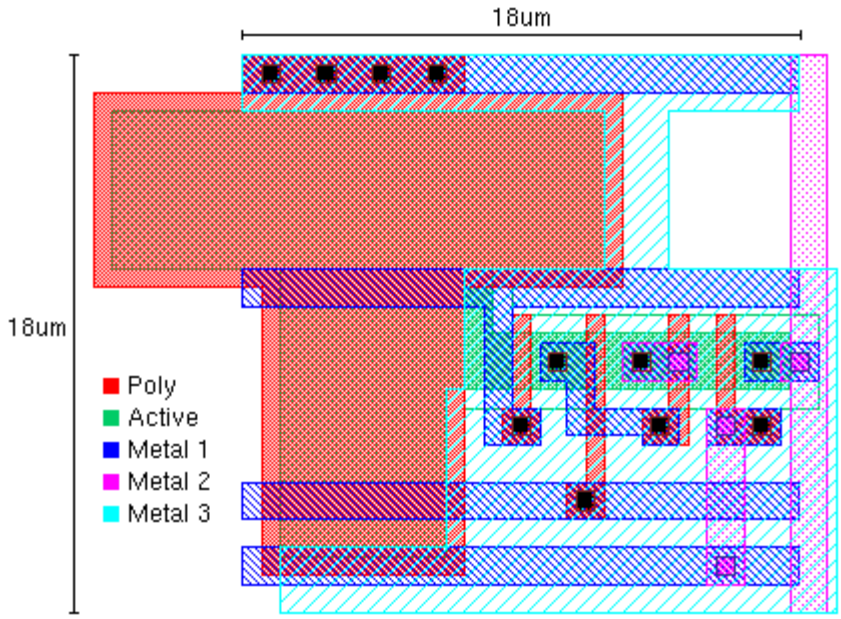

Figure 6 - CMOS photogate APS layout, using a double poly, three metal CMOS process

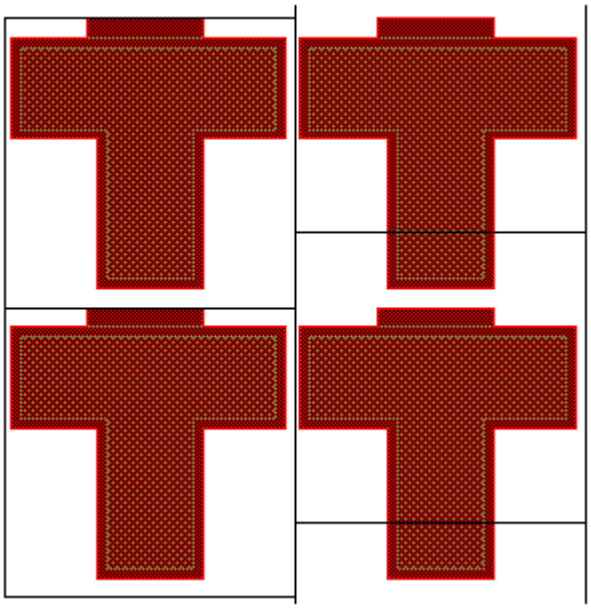

Figure 7 - DOE unit overlap of pixels

5. NOISE SUPPRESSION

For an APS, FPN must be suppressed or the performance of the sensor will be limited. [24] A light shield has been used as described to limit cross talk between pixels, but the primary sources of FPN will be reset voltage variations between pixels and column-to-

column variation resulting from the column readout structure. Two techniques for FPN suppression have been implemented.

5.1 Correlated Double Sampling

CDS is a method for suppressing reset noise. A schematic for a basic readout circuit with CDS is shown in Figure 8. CDS first samples the reset voltage of a pixel and then samples the signal voltage. The difference between the two is the output voltage. CDS suppresses reset noise from variations in reset voltage between pixels as well as threshold variations from the source follower transistor within the pixel. [13] CDS also reduces low frequency noise.

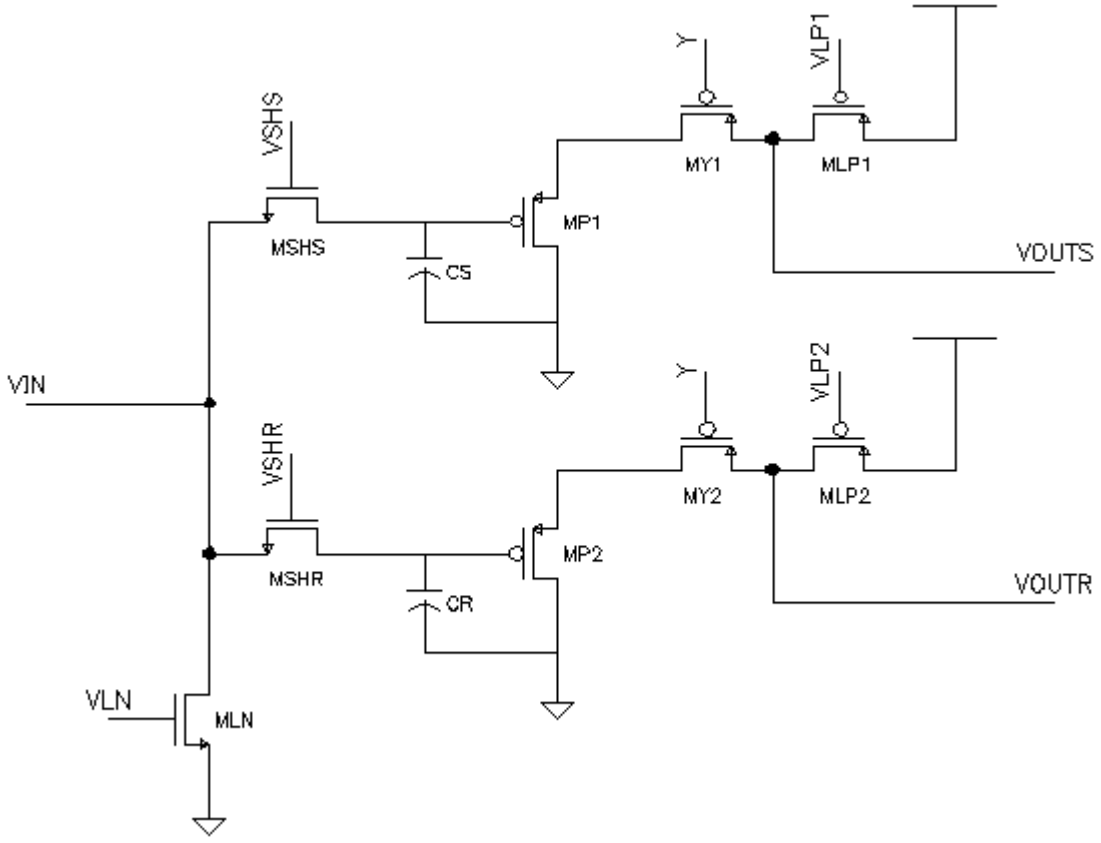

Figure 8 - Schematic of CDS circuit

5.2 Column Reference Subtraction

To correct for column-to-column variations caused by the column readout structure, a row of dark reference pixels is added to the sensor array, completely covered by the light shield. This row is read out in the same manner as the normal pixels. In the signal processing stage, which occurs after analog to digital conversion, this row is subtracted from each of the other rows, serving as a column reference. For this reason, this row

should be read out first, so that column reference subtraction can occur before the polarization-sum and polarization-difference are formed.

6. OPERATION

Control circuits for this camera have not been designed, but are relatively straightforward. The power rail, VDD, is carried on the light shield layer that covers the entire array and is set to 5 volts. The transfer gate within the pixel, TX, is set to 2.5 volts, the gate of transistor MLN is biased at 1.5 volts, and the gates of MLP1 and MLP2 are biased at 2.5 volts. (See Figure 7) The first period for operation is the signal integration period, during which the photogate (PG) is biased at 5 volts. The reset transistor, MR, is biased at 2.5 volts as an antiblooming drain. Row select switches are off. After signal integration, the sensor array should be read out row by row. The row to be read out is selected by enabling the row select switch, MS. Then, the reset transistor is pulsed to 5 volts in order to reset the floating diffusion node of the pixel (FD). The reset voltage is then sampled by selecting the sample-and-hold switch MSHR. This stores the reset voltage on capacitor CR. The photogate is then pulsed low to 0 volts, which transfers the signal charge to the floating diffusion node. The signal voltage is sampled by selecting the sample-and-hold switch MSHS. This stores the signal voltage on capacitor CS. Setting the column-select switches MY1 and MY2 low scans out the stored reset and signal voltages. A partial timing sequence is shown in Figure 9.

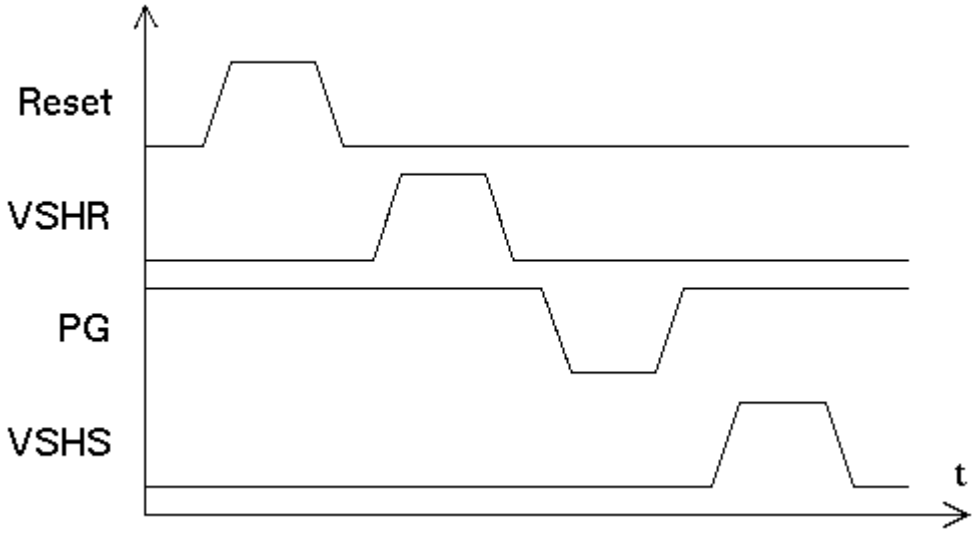

Figure 9 - Timing for pixel and read out operation

7. INTENSITY SCALING

Because the DOE does not function as an ideal polarization analyzer, corrective intensity scaling is necessary to obtain the true components of linear polarization. The intensity of output light from a DOE is different for transverse electric (TE) waves and transverse magnetic (TM) waves. The ratio of TE to TM for an ideal polarization analyzer is 1 to 0.

Additional scaling of the intensities to enhance PDI performance for specific environments is also desirable. A combined method for corrective scaling is presented below.

The intensities of orthogonal components of incoming light are symbolized as the vector *T*, the output intensities from paired pixels as the vector *N*, and the polarization-difference image as the vector *P*.

$$N = [I_1\ I_2]^T \quad (2)$$
$$T = [TE\ TM]^T \quad (3)$$
$$P = [PS\ PD]^T \quad (4)$$

If the DOE is exposed to purely TE and TM waves, the ratio c_1/c_2 is the peak intensity on the focal plane for a TE versus a TM wave. This ratio forms the scaling matrix C, and scaling factors s_1, s_2, d_1, d_2, used for PDI performance enhancement, form the scaling matrix K. The matrix A is the final scaling matrix to be applied in the signal processing stage of the camera. Note that if the DOE is ideal, C is equal to the identity matrix as expected.

$$C = [[c_1\ c_2][c_2\ c_1]] \quad (5)$$
$$K = [[s_1\ s_2][d_1\ -d_2]] \quad (6)$$
$$A = [[a_1\ a_2][b_1\ b_2]] \quad (7)$$

The output intensity vector, *N*, is equal to the DOE ratio matrix multiplied by the ideal intensity vector. The PDI is equal to the performance scaling matrix multiplied by the ideal intensity vector as well as the final scaling matrix multiplied by the output intensity vector.

$$N = CT \quad (8)$$
$$P = KT \quad (9)$$
$$P = AN \quad (10)$$

These relationships give the final scaling matrix as

$$A = KC^{-1} \quad (11a)$$
$$A = [[(s_1c_1 - s_2c_2)\ \ (s_2c_1 - s_1c_2)][(d_1c_1 + d_2c_2)\ \ -(d_2c_1 + d_1c_2)]] / (c_1^2 - c_2^2) \quad (11b)$$

This gives the PDI as

$$_{PS}I = [(s_1c_1 - s_2c_2)\ I_1 + (s_2c_1 - s_1c_2)\ I_2] / (c_1^2 - c_2^2) \quad (12a)$$
$$_{PD}I = [(d_1c_1 + d_2c_2)\ I_1 - (d_2c_1 + d_1c_2)\ I_2] / (c_1^2 - c_2^2) \quad (12b)$$

Because both the PS and PD will be scaled with an affine transform to use the full range of intensity and color values, and the ratio of c_1/c_2 is fixed for the entire array, the PDI can be simplified to

$$_{PS}I = (s_1c_1 - s_2c_2)\, I_1 + (s_2c_1 - s_1c_2)\, I_2 \qquad (13a)$$
$$_{PD}I = (d_1c_1 + d_2c_2)\, I_1 - (d_2c_1 + d_1c_2)\, I_2 \qquad (13b)$$

These equations can be easily implemented in a digital device for the purposes of a polarization-difference camera. Note that if the polarization analyzer is ideal and no corrective scaling occurs, Equations 13a and 13b are identical to Equations 1a and 1b.

8. EXPERIMENTAL RESULTS

Simulations have been done to test the designs for the APS and readout circuitry. Because control and analog to digital conversion components of the camera have not been designed, the array has yet to be fabricated. All simulations were done with AMI 0.6µm process technology parameters for SPICE.

8.1 APS

To test basic operation of the pixel, the photocurrent used to simulate the photogate was varied from 50 pA to 300 pA in steps of 50 pA while the reset and select transistors were operated in a simplified manner. This corresponds to a variation in current per unit area from 0.38 pA/µm^2 to 2.3 pA/µm^2. The reset transistor was initially pulsed, and then the select was enabled. Line and photogate capacitance were modeled with capacitors. Information about the specific simulation parameters is included in Appendix A. Figure 10 shows the voltage at the output node during operation for each photocurrent.

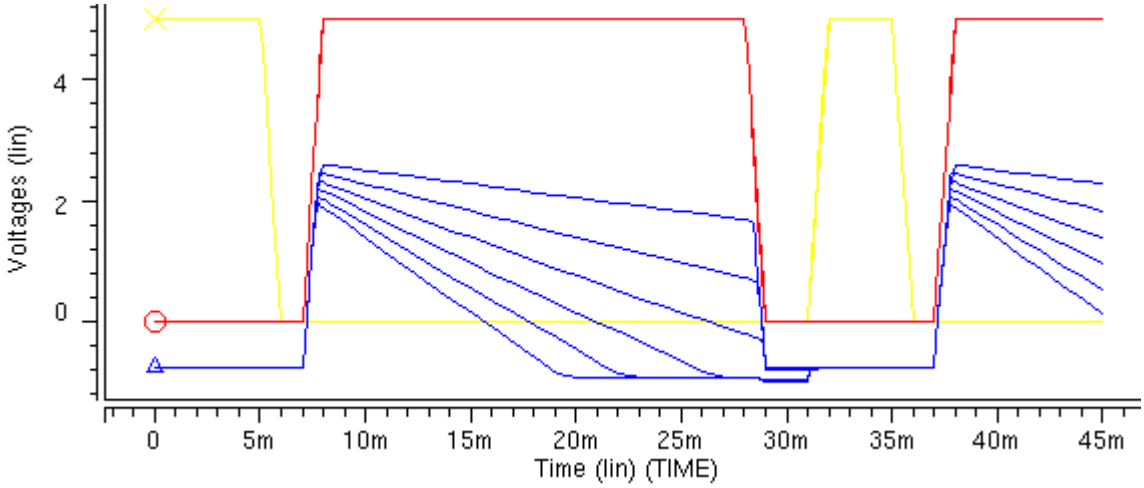

Figure 10 - SPICE simulation of APS

8.2 Readout Circuit

The operation of the readout circuit was tested using a simplified model of half of the circuit. This simplification accurately models final operation, since the reset and signal halves of the readout circuit are identical. The line voltage was varied from 0 to 4 volts and stepped by 0.25 volts. The line voltage was sampled onto a capacitor by enabling the sample-and-hold switch. The voltage was then read out by enabling the column select

switch. Information about the specific simulation parameters is included in Appendix B. Figure 11 shows the output voltage during operation.

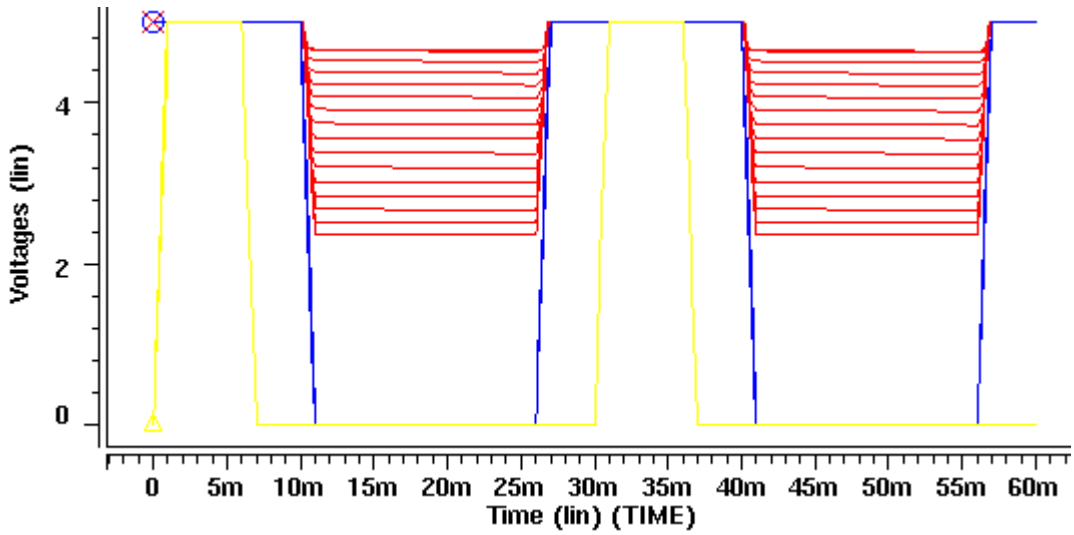

Figure 11 - SPICE simulation of readout

9. DISCUSSION AND CONCLUSIONS

PDI is a method for extracting polarization information from a scene. PDI has also been demonstrated as an effective technique for improving target detection in scattering media. A real-time polarization-difference camera that was portable and capable of low power usage would be useful for many applications. Designs for CMOS APSs and readout circuits have been presented, along with a corrective scaling methodology to compensate for non-ideal diffractive optical element polarization analyzers.

A CMOS APS was designed and simulated for use in the polarization-difference camera. The simulation yielded good results. The pixel was subsequently laid out to fit with the diffractive optical element polarization analyzer and maximize the detector area. A methodology for operating the pixel was also presented.

Readout circuitry for row-based readout was also designed and simulated for use in the camera. This simulation also yielded good results. Readout circuitry included CDS to reduce fixed pattern noise. A row of dark pixels will be added to the array to serve as a column reference in the signal processing stage.

A corrective scaling technique was demonstrated to compensate for the non-ideal diffractive optical element polarization analyzer. This technique can also be used to introduce performance related scaling factors if desired. This process is to be included in the signal processing stage.

10. RECOMMENDATIONS

While significant progress has been made this summer, this project is not yet complete. The readout circuit still must be laid out, though space considerations are not as important as for the pixel. In addition, both the pixel and the readout circuit should be simulated with actual values from the layout, including parasitic effects. Design and testing of the control and drive electronics still remains to be done, as well as the design of an analog to digital converter. Once those stages are complete, the camera chip can be fabricated and combined with the DOE for testing.

The signal processing stage, including corrective scaling, polarization-sum, and polarization-difference, should in implemented in a separate device. A field programmable gate array would be appropriate, though the digital output of the camera chip allows for some flexibility.

11. ACKNOWLEDGMENTS

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12. REFERENCES

1. S. Portonovo, Components of a CMOS imager for a polarization-difference camera, *SUNFEST 2000, NSF Technical Report TR-CST22DEC00*, University of Pennsylvania, pp. 200-245.
2. M.P. Rowe, E.N. Pugh, Jr., J.S. Tyo, and N. Engheta, Polarization-difference imaging: a biologically inspired technique for imaging in scattering media, *Optics Letters*, 20 (1995) 608-610.
3. M.P. Rowe, N. Engheta, S.S. Easter, Jr., and E.N. Pugh, Jr., Graded-index model of a fish double cone exhibits differential polarization sensitivity, *J. Opt. Soc. Am. A*, 11 (1994) 55-70.
4. J.S. Tyo, M.P. Rowe, E.N. Pugh, Jr., and N. Engheta, Target detection in optically scattering media by polarization-difference imaging, *Applied Optics*, 35 (1996) 1855-1870.
5. L.B. Wolff and T.A. Mancini, Liquid crystal polarization camera, *IEEE Transactions on Robotics and Automation*, 13 (1997) 195-203.
6. L.B. Wolff, Applications of polarization camera technology, *IEEE Expert*, October 1995, pp. 30-38.
7. Z.K. Kalayjian, *VLSEye: Optoelectronic Vision and Image Processing*, Doctoral dissertation, The John Hopkins University, 1999.

8. J.S. Tyo, E.N. Pugh, Jr., and N. Engheta, Colorimetric representations for use with polarization-difference imagine of objects in scattering media, *J. Opt. Soc. Am. A*, 15 (1998) 367-374.
9. E.R. Fossum, CMOS image sensors: electronic camera on a chip, *International Electron Devices Meeting, Washington, D.C., USA, Dec. 1995*, pp. 17-25.
10. M. Ferstl and R. Steingruber, Commercial fabrication of micro-structures and micro-optical elements for research and industrial applications, *Heinrich-Hertz-Institut fur Nachrichtentechnik Berlin GmbH, Annual Report 1998*, pp. 109-112.
11. J.N Mait, A. Scherer, O. Dial, D.W. Prather, and X. Gao, Diffractive lens fabricated with binary features less than 60 nm, *Optics Letters*, 25 (2000) 381-383.
12. A. Moini, *Vision Chips or Seeing Silicon*, The University of Adelaide, Adelaide, 3rd revision, March 1997, pp. 133-135, 155-162.
13. S.K. Mendis, S.E. Kemeny, R.C. Gee, B. Pain, C.O. Staller, Q. Kim, and E.R. Fossum, CMOS active pixel image sensors for highly integrated imaging systems, *IEEE Journal of Solid-State Circuits*, 32 (1997) 187-197.
14. R.H. Nixon, S.E. Kemeny, B. Pain, C.O. Staller, and E.R. Fossum, 256x256 CMOS active pixel sensor camera-on-a-chip, *IEEE Journal of Solid-State Circuits*, 31 (1996) 2046-2050.
15. B. Mansoorian, H.-Y. Yee, S. Huang, and E. Fossum, A 250mW, 60Frames/s 1280x720 pixel 9b CMOS digital image sensor, *IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, Feb. 1999*, pp. 312-313.
16. A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E.R. Fossum, A high speed, 500 frames/s, 1024x1024 CMOS active pixel sensor, *IEEE Symposium on VLSI Circuits, Kyoto, Japan, June 1999*, pp. 137-138.
17. T. Hamamoto and K. Aizawa, A computational image sensor with adaptive pixel-based integration time, *IEEE Journal of Solid-State Circuits*, 36 (2001) 580-585.
18. Z. Zhou, B. Pain, and E.R. Fossum, CMOS active pixel sensor with on-chip successive approximation analog-to-digital converter, *IEEE Transactions on Electron Devices*, 44 (1997) 1759-1763.
19. J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, and E. Fossum, On-focal-plane signal processing for current-mode active pixel sensors, *IEEE Transactions on Electron Devices*, 44 (1997) 1747-1758.
20. C.H. Aw and B.A. Wooley, A 128x128-pixel standard-CMOS image sensor with electronic shutter, *IEEE Journal of Solid-State Circuits*, 31 (1996) 1922-1930.
21. K. Yonemoto, H. Sumi, R. Suzuki, and T. Ueno, A CMOS image sensor with a simple FPN-reduction technology and a hole accumulated diode, *IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, Feb. 2000*, pp. 102-103.
22. J. Coulombe, M. Sawan, and C. Wang, Variable resolution CMOS current mode active pixel sensor, *IEEE International Symposium on Circuits and Systems, Geneva, Switzerland, May 2000*, pp. 293-296.
23. Y. Shih and C. Wu, The design of high-performance 128x128 CMOS image sensors using new current-readout techniques, *IEEE International Symposium on Circuits and Systems, Albuquerque, New Mexico, USA, Nov.1999*, pp. 168-171.
24. H. Tian, B. Fowler, and A. El Gamal, Analysis of temporal noise in CMOS photodiode active pixel sensor, *IEEE Journal of Solid-State Circuits*, 36 (2001) 92-101.

APPENDIX A

SPICE Source Code – Active Pixel Sensor
AMI 0.6μm n-well CMOS transistors

```
* Active Pixel Sensor

VDD VDD! 0 DC 5v

VRESET          R 0  PULSE 5.0 0.0 5E-3 1E-3 1E-3 25E-3 30E-3
VSELECT         S 0  PULSE 0.0 5.0 7E-3 1E-3 1E-3 20E-3 30E-3

IBIAS    VOUT 0  DC=10E-6
IPHOTO          FD   0  DC=0.0

CLINE   VOUT 0  500E-15
CDIODE          FD   0  1E-12

MX BTWN S VOUT 0  AMI06N  L=600E-9 W=3E-6 AD=4.5E-12 AS=4.5E-12 PD=9E-6
+PS=9E-6 M=1
MIN VDD! FD BTWN 0  AMI06N  L=600E-9 W=3E-6 AD=4.5E-12 AS=4.5E-12 PD=9E-6
+PS=9E-6 M=1
MR VDD! R FD 0  AMI06N  L=600E-9 W=3E-6 AD=4.5E-12 AS=4.5E-12 PD=9E-6 PS=9E-6
+M=1

.MODEL AMI06N NMOS ( LEVEL=49 VERSION=3.1 TNOM=27 TOX=1.41E-8 XJ=1.5E-7
+NCH=1.7E17 VTH0=0.7086 K1=0.8354582 K2=-8.84310000E-02 K3=41.4403818
+K3B=-1.40000000E+01 W0=6.480766E-7 NLX=1E-10 DVT0W=0 DVT1W=5.3E6
+DVT2W=-3.20000000E-02 DVT0=3.6139113 DVT1=0.3795745 DVT2=-1.39997600E-01
+U0=533.6953445 UA=7.558023E-10 UB=1.181167E-18 UC=2.582756E-11 VSAT=1.300981E5
+A0=0.5292985 AGS=0.1463715 B0=1.283336E-6 B1=1.408099E-6 KETA=-1.73166000E-02
+A1=0 A2=1 RDSW=2.268366E3 PRWG=-1.00000000E-03 PRWB=6.320549E-5 WR=1
+WINT=2.043512E-7 LINT=3.034496E-8 XL=0 XW=0 DWG=-1.44614900E-08
+DWB=2.077539E-8 VOFF=-1.13722600E-01 NFACTOR=1.2880596 CIT=0 CDSC=1.506004E-4
+CDSCD=0 CDSCB=0 ETA0=3.815372E-4 ETAB=-1.02917800E-03 DSUB=2.173055E-4
+PCLM=0.6171774 PDIBLC1=0.185986 PDIBLC2=3.473187E-3 PDIBLCB=-1.00000000E-03
+DROUT=0.4037723 PSCBE1=5.998012E9 PSCBE2=3.788068E-8 PVAG=0.012927 DELTA=0.01
+MOBMOD=1 PRT=0 UTE=-1.50000000E+00 KT1=-1.10000000E-01 KT1L=0 KT2=0.022
+UA1=4.31E-9 UB1=-7.61000000E-18 UC1=-5.60000000E-11 AT=3.3E4 WL=0 WLN=1 WW=0
+WWN=1 WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0 CAPMOD=2 XPART=0.4 CGDO=1.99E-10
+CGSO=1.99E-10 CGBO=0 CJ=4.233802E-4 PB=0.9899238 MJ=0.4495859
+CJSW=3.825632E-10 PBSW=0.1082556 MJSW=0.1083618 PVTH0=0.0212852
+PRDSW=-1.61546703E+01 PK2=0.0253069 WKETA=0.0188633 LKETA=0.0204965       )

.TRAN .2ms 45ms SWEEP IPHOTO 50pa 300pa 50pa
.TEMP    25.0000
.OP
.SAVE
.OPTION POST
.END
```

APPENDIX B

SPICE Source Code – Readout Circuit Simulation
AMI 0.6μm n-well CMOS transistors

```
* Column readout circuit

.GLOBAL VDD!
VDD VDD! 0 DC 5V

VLN VLN 0  1.5
VLP VLP 0  2.5
VIN COLBUS 0 dc 0v
VSH SH 0  PULSE (0V 5V 0ms 1ms 1ms 5ms 30ms)
VY  Y 0  PULSE (5V 0V 10ms 1ms 1ms 15ms 30ms)

COUT VOUT 0  1E-12 M=1.0
CS SIGNAL 0  1E-12 M=1.0

MP 0 SIGNAL BTWN VDD!  AMI06P  L=600E-9 W=72E-6 AD=108E-12 AS=108E-12
+PD=147E-6 PS=147E-6 M=1
MY BTWN Y VOUT VDD!  AMI06P  L=600E-9 W=72E-6 AD=108E-12 AS=108E-12
+PD=147E-6 PS=147E-6 M=1
MLP VOUT VLP VDD! VDD!  AMI06P  L=600E-9 W=18E-6 AD=27E-12 AS=27E-12
+PD=39E-6 PS=39E-6 M=1

MSH SIGNAL SH COLBUS 0  AMI06N  L=1.05E-6 W=1.5E-6 AD=2.25E-12 AS=2.25E-12
+PD=6E-6 PS=6E-6 M=1
MLN COLBUS VLN 0 0  AMI06N  L=1.95E-6 W=1.5E-6 AD=2.25E-12 AS=2.25E-12 PD=6E-6
+PS=6E-6 M=1

.MODEL AMI06N NMOS ( LEVEL=49 VERSION=3.1 TNOM=27 TOX=1.41E-8 XJ=1.5E-7
+NCH=1.7E17 VTH0=0.7086 K1=0.8354582 K2=-8.84310000E-02 K3=41.4403818
+K3B=-1.40000000E+01 W0=6.480766E-7 NLX=1E-10 DVT0W=0 DVT1W=5.3E6
+DVT2W=-3.20000000E-02 DVT0=3.6139113 DVT1=0.3795745 DVT2=-1.39997600E-01
+U0=533.6953445 UA=7.558023E-10 UB=1.181167E-18 UC=2.582756E-11 VSAT=1.300981E5
+A0=0.5292985 AGS=0.1463715 B0=1.283336E-6 B1=1.408099E-6 KETA=-1.73166000E-02
+A1=0 A2=1 RDSW=2.268366E3 PRWG=-1.00000000E-03 PRWB=6.320549E-5 WR=1
+WINT=2.043512E-7 LINT=3.034496E-8 XL=0 XW=0 DWG=-1.44614900E-08
+DWB=2.077539E-8 VOFF=-1.13722600E-01 NFACTOR=1.2880596 CIT=0 CDSC=1.506004E-4
+CDSCD=0 CDSCB=0 ETA0=3.815372E-4 ETAB=-1.02917800E-03 DSUB=2.173055E-4
+PCLM=0.6171774 PDIBLC1=0.185986 PDIBLC2=3.473187E-3 PDIBLCB=-1.00000000E-03
+DROUT=0.4037723 PSCBE1=5.998012E9 PSCBE2=3.788068E-8 PVAG=0.012927 DELTA=0.01
+MOBMOD=1 PRT=0 UTE=-1.50000000E+00 KT1=-1.10000000E-01 KT1L=0 KT2=0.022
+UA1=4.31E-9 UB1=-7.61000000E-18 UC1=-5.60000000E-11 AT=3.3E4 WL=0 WLN=1 WW=0
+WWN=1 WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0 CAPMOD=2 XPART=0.4 CGDO=1.99E-10
+CGSO=1.99E-10 CGBO=0 CJ=4.233802E-4 PB=0.9899238 MJ=0.4495859
+CJSW=3.825632E-10 PBSW=0.1082556 MJSW=0.1083618 PVTH0=0.0212852
+PRDSW=-1.61546703E+01 PK2=0.0253069 WKETA=0.0188633 LKETA=0.0204965       )



.MODEL AMI06P PMOS ( LEVEL=49 VERSION=3.1 TNOM=27 TOX=1.41E-8 XJ=1.5E-7
+NCH=1.7E17 VTH0=-9.17995200E-01 K1=0.5575604 K2=0.010265 K3=14.0655075
```

```
+K3B=-2.30329210E+00 W0=1.147829E-6 NLX=1.114768E-10 DVT0W=0 DVT1W=5.3E6
+DVT2W=-3.20000000E-02 DVT0=2.2896412 DVT1=0.5213085 DVT2=-1.33798700E-01
+U0=202.4540953 UA=2.290194E-9 UB=9.779742E-19 UC=-3.69771000E-11
+VSAT=1.307891E5 A0=0.8356881 AGS=0.1568774 B0=2.365956E-6 B1=5E-6
+KETA=-5.76932800E-03 A1=0 A2=1 RDSW=2.746814E3 PRWG=2.34865E-3 PRWB=0.0172298
+WR=1 WINT=2.586255E-7 LINT=7.205014E-8 XL=0 XW=0 DWG=-2.13305400E-08
+DWB=9.857534E-9 VOFF=-8.37499000E-02 NFACTOR=1.2415529 CIT=0 CDSC=4.363744E-4
+CDSCD=0 CDSCB=0 ETA0=0.11276 ETAB=-2.94840000E-03 DSUB=0.3389402
+PCLM=4.9847806 PDIBLC1=2.481735E-5 PDIBLC2=0.01 PDIBLCB=0 DROUT=0.9975107
+PSCBE1=3.497872E9 PSCBE2=4.974352E-9 PVAG=10.9914549 DELTA=0.01 MOBMOD=1 PRT=0
+UTE=-1.50000000E+00 KT1=-1.10000000E-01 KT1L=0 KT2=0.022 UA1=4.31E-9
+UB1=-7.61000000E-18 UC1=-5.60000000E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1 WWL=0
+LL=0 LLN=1 LW=0 LWN=1 LWL=0 CAPMOD=2 XPART=0.4 CGDO=2.4E-10 CGSO=2.4E-10
+CGBO=0 CJ=7.273568E-4 PB=0.9665597 MJ=0.4959837 CJSW=3.114708E-10 PBSW=0.99
+MJSW=0.2653654 PVTH0=9.420541E-3 PRDSW=-2.31257157E+02 PK2=1.396684E-3
+WKETA=1.862966E-3 LKETA=5.728589E-3     )

.TRAN .1ms 60ms sweep VIN 0V 4V .25V
.TEMP    25.0000
.OP
.save
.OPTION POST
.END
```

APPENDIX C

CIF Output – APS
AMI 0.6μm n-well process
Use scale = 0.033333333 for Cadence

(CIF file written on 31-Jul-2001 15:38:33 by CADENCE);
DS 1 3 1;
9 PIXEL;
L CMT;P 0,540 540,540 540,486 414,486 414,333 576,333 576,0 36,0 36,63 198,63 198,216 216,216 216,333 351,333 351,486 0,486;L CSN;P 216,36 216,198 558,198 558,288 261,288 261,315 369,315 369,504 -144,504 -144,315 18,315 18,36;L CAA;
P 351,486 351,333 243,333 243,270 531,270 531,216 198,216 198,54 36,54 36,333 -126,333 -126,486;L CVA;B 18 18 468,180;B 18 18 423,243;B 18 18 540,243;
B 18 18 468,45;L CCC;B 18 18 387,243;B 18 18 306,243;B 18 18 333,108;
B 18 18 405,180;B 18 18 504,180;B 18 18 504,243;B 18 18 270,180;B 18 18 27,522;
B 18 18 81,522;B 18 18 135,522;B 18 18 189,522;L CPG;P 459,288 459,162 522,162 522,198 477,198 477,288;P 351,288 351,90 315,90 315,126 333,126 333,288;
P 432,288 432,162 387,162 387,198 414,198 414,288;P 369,315 369,504 216,504 216,540 0,540 0,504 -144,504 -144,315 18,315 18,36 216,36 216,315;P 279,288 279,198 288,198 288,162 252,162 252,198 261,198 261,288;L CMF;B 72 36 486,180;
P 288,261 342,261 342,198 423,198 423,162 387,162 387,171 315,171 315,225 288,225;B 540 36 270,45;B 540 36 270,108;B 72 36 522,243;B 72 36 405,243;
B 540 36 270,522;P 0,297 234,297 234,162 288,162 288,198 261,198 261,297 540,297 540,333 0,333;L CMS;P 567,0 567,540 531,540 531,261 522,261 522,225 531,225 531,0;P 450,27 486,27 486,198 450,198;B 72 36 405,243;
DF;
C 1;
E