



# AMPLIFICATION CIRCUITS AND PATTERNING METHODS OF ORGANIC FIELD-EFFECT TRANSISTORS

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# **Organic Field-Effect Transistors**

•Doped Si bottom gate and SiO2 dielectric layer

•Pentacene semiconductor

•Self-Assembled Molecules on source and drain for ambipolar characteristics

•Mobility around 0.25cm2/Vs

•Maximum drain currents near 30µA





# Background

•OFETs hold great promise for the future of brain-computer interfaces

- •Conformal
- •Small feature size
- •Greater neural selectivity
- •Devices placed directly on surface rather than wired

#### •Current techniques

- •3mm diameter sensors
- •1cm spacing between sensors
- •Around 150,000 neurons/mm2
- •Bulky wire arrays attaching to machinery

J.J. Van Gompel, G.A. Worrell, M.L. Bell, T.A. Patrick, G.D. Cascino and C. Raffel et al., Intracranial Electroencephalography with Subdural Grid Electrodes: Techniques, Complications, and Outcomes, *Neurosurgery*, 63 (2008) 498–505.





# What needs to be done

•Amplification

- •Brain signals are very low voltage, order of microvolts
- •Need to amplify these signals for use in electronics
- •Organic transistors can be made in amplifying configuration





# What needs to be done

•Patterning via holes

•Brain is in aqueous environment

•Parylene can serve as encapsulant for devices

•Parylene can also act as a dielectric between transistor and sensor

•Electrodes must be placed from sensor in brain to gate

•Holes must be etched through parylene and transistor layers to make this connection





# **FET Amplifiers**



- •Transistors in amplifying topology can generate "small signal" gain
  - •DC voltage applied to gate
  - •Transistor, in saturation, draws drain current
  - •Small perturbation of gate voltage (AC signal) causes corresponding small change in drain current
  - •Take advantage of this drain current oscillation





# Common Source Amplifier

#### •Source is grounded

Drain is connected to power supply by resistorSmall drain current perturbation now causes a small voltage signal at the drain

•Amount of gain is determined by the device characteristics, resistance, and DC biasing



# **Common Source Amplifier Calculations**

 $|Gain| = g_m R_d = \mu C_{ox} (|V_{gs}| - |V_t|) R_d$ 



#### •Used constant mobility and threshold voltage



### **DC** Analysis Gain Predictions





# Small Signal Gain Results



•Used 1Vpp small signal input at 15Hz

•About half as much as calculated; only slightly less than DC prediction







- •-3dB point near 35Hz
- •Higher frequencies severely limited gain due to high gate capacitance
- •Rolls off greater than -20dB/decade



# Further Investigation

•Why calculations were off (determining how mobility and threshold voltages change with gate voltage)

•Different amplifying circuits to take advantage of ambipolar characteristics



Ambipolar active load



# **Patterning Methods**

Parylene was etched using oxygen plasma
Glass and silicon substrates measured well on profilometer
100W, 500mTorr showed a rate of 0.2µm/minute
Kapton samples gave no decent measurements

BCB and spin-on-glass were etched with SF6
Spin-on-glass did not exhibit etching with O2
SF6 etching did not give any consistent results
BCB results could not yet be measured



## Further Investigation

#### •Using polyimide to avoid SoG and Kapton etching problems



•Attempt etching using photoresist in hole pattern, then test with deposited electrode

H. Kawaguchi, T. Sakurai, High Mobility of Pentacene Field-Effect Transistors with Polyimide Gate Dielectric Layers, *Appl. Phys. Lett.*, 84 (2004) 3789-3791.





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