AMPLIFICATION CIRCUITS AND PATTERNING METHODS OF ORGANIC FIELD-EFFECT TRANSISTORS

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Organic Field-Effect Transistors

• Doped Si bottom gate and SiO2 dielectric layer
• Pentacene semiconductor
• Self-Assembled Molecules on source and drain for ambipolar characteristics
• Mobility around 0.25 cm²/Vs
• Maximum drain currents near 30 μA
Background

• OFETs hold great promise for the future of brain-computer interfaces
  • Conformal
  • Small feature size
  • Greater neural selectivity
  • Devices placed directly on surface rather than wired

• Current techniques
  • 3mm diameter sensors
  • 1cm spacing between sensors
  • Around 150,000 neurons/mm²
  • Bulky wire arrays attaching to machinery

What needs to be done

• Amplification
  • Brain signals are very low voltage, order of microvolts
  • Need to amplify these signals for use in electronics
  • Organic transistors can be made in amplifying configuration
What needs to be done

- Patterning via holes
  - Brain is in aqueous environment
  - Parylene can serve as encapsulant for devices
  - Parylene can also act as a dielectric between transistor and sensor
  - Electrodes must be placed from sensor in brain to gate
  - Holes must be etched through parylene and transistor layers to make this connection
• Transistors in amplifying topology can generate “small signal” gain
  • DC voltage applied to gate
  • Transistor, in saturation, draws drain current
  • Small perturbation of gate voltage (AC signal) causes corresponding small change in drain current
  • Take advantage of this drain current oscillation
Common Source Amplifier

- Source is grounded
- Drain is connected to power supply by resistor
- Small drain current perturbation now causes a small voltage signal at the drain
- Amount of gain is determined by the device characteristics, resistance, and DC biasing
Common Source Amplifier Calculations

\[ |Gain| = g_m R_d = \mu C_{ox} (|V_{gs}| - |V_t|) R_d \]

- Used constant mobility and threshold voltage
DC Analysis Gain Predictions

<table>
<thead>
<tr>
<th>Drain Resistance</th>
<th>Slope</th>
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</thead>
<tbody>
<tr>
<td>4.7MΩ</td>
<td>-1.599</td>
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<tr>
<td>6.9MΩ</td>
<td>-2.161</td>
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<td>10MΩ</td>
<td>-2.695</td>
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<td>-3.08</td>
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<td>-4.349</td>
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<td>50MΩ</td>
<td>-4.319</td>
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</table>
Small Signal Gain Results

- Used 1Vpp small signal input at 15Hz
- About half as much as calculated; only slightly less than DC prediction
• -3dB point near 35Hz
• Higher frequencies severely limited gain due to high gate capacitance
• Rolls off greater than -20dB/decade
Further Investigation

• Why calculations were off (determining how mobility and threshold voltages change with gate voltage)

• Different amplifying circuits to take advantage of ambipolar characteristics

Ambipolar active load
Patterning Methods

- Parylene was etched using oxygen plasma
  - Glass and silicon substrates measured well on profilometer
  - 100W, 500mTorr showed a rate of 0.2μm/minute
  - Kapton samples gave no decent measurements

- BCB and spin-on-glass were etched with SF6
  - Spin-on-glass did not exhibit etching with O2
  - SF6 etching did not give any consistent results
  - BCB results could not yet be measured
Further Investigation

• Using polyimide to avoid SoG and Kapton etching problems

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